



AiP16C22

Ram Mapping 44 Seg×4 Com LCD Driver and Controller with 2-Line Serial Interface

Product Specification

Specification Revision History:

Version	Date	Description
2020-07-A1	2020-07	New
2024-07-B1	2024-07	Update the template; modify the content



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1、General Description

AiP16C22 is a kind of LCD controller/driver .The device provides a display mode: 1/4 duty display mode. The display segments of the device are 176 patterns (44×4, LQFP52) or 160 patterns (40×4, LQFP48). AiP16C22 has a built-in clock generator, LCD bias voltage generation module, LCD drive voltage follower and standard I²C interface.

Features:

- Operating voltage: 2.4 to 5.5V
- I²C interface
- Low power consumption
- Versatile blinking modes
- Internal clock generator
- Display Mode:
 - LQFP52:
44×4 patterns: 44 SEG and 4 COM
 - LQFP48:
40×4 patterns: 40 SEG and 4 COM
- Bias: 1/2 or 1/3
- Duty: 1/4
- Internal LCD bias generator with voltage follower
- LCD drive voltage can be adjusted by external resistor
- V_{LCD} voltage adjustable
- Two selectable LCD frame frequencies: 80Hz or 160Hz
- Packaging information: LQFP48/LQFP52

Ordering Information:

Tube packing specifications:

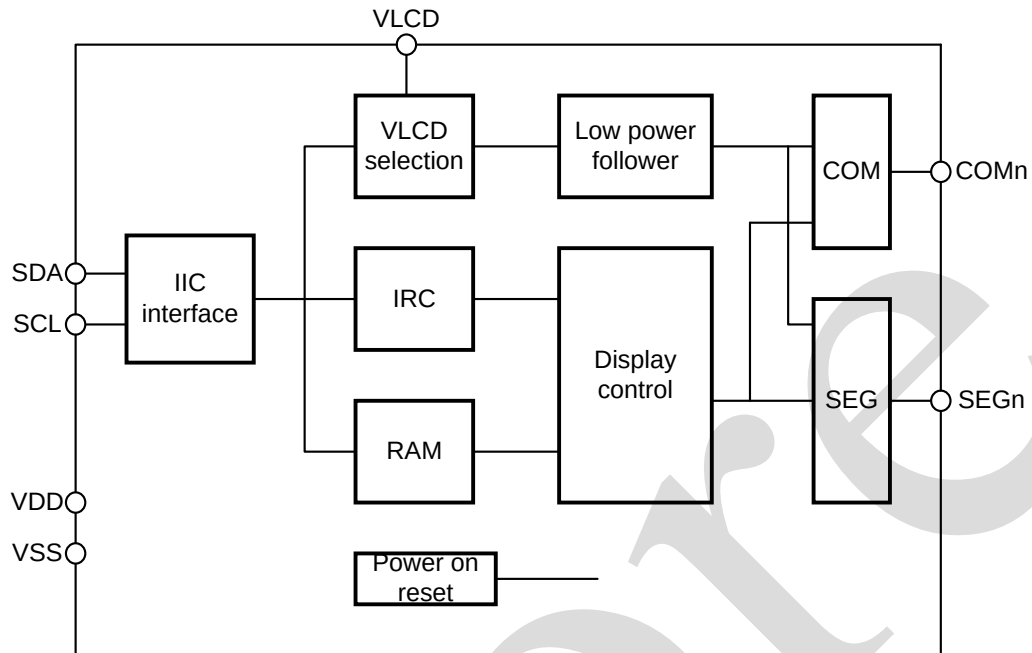
Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP16C22LA48.TB	LQFP48	AiP16C22	250 PCS/plate	10 plate/box	2500 PCS/box	Dimensions of plastic enclosure: 7.0mm×7.0mm Pin spacing: 0.5mm
AiP16C22LD52.TB	LQFP52	AiP16C22	90 PCS/plate	10 plate/box	900 PCS/box	Dimensions of plastic enclosure: 14.0mm×14.0mm Pin spacing: 1.0mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

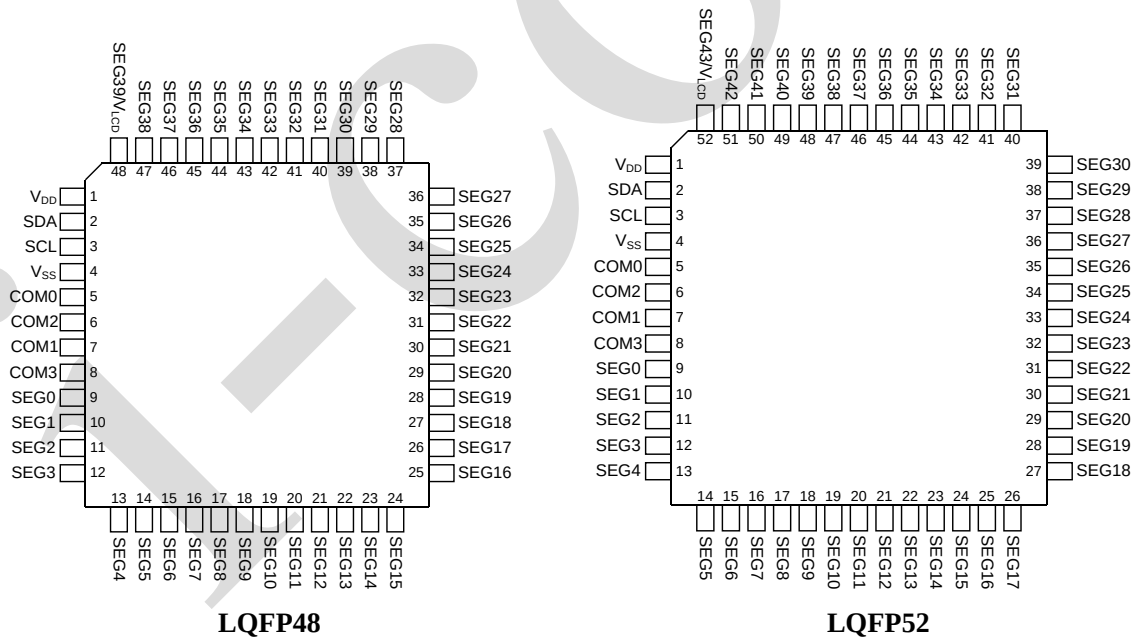


2、Block Diagram And Pin Description

2.1、Block Diagram



2.2、Pin Configurations





2.3、Pin Description

Pin No.		Pin Name	Type	Description
LQFP48	LQFP52			
2	2	SDA	I/O	Serial data input/output for I ² C interface
3	3	SCL	I	Serial clock input for I ² C interface
1	1	V _{DD}	-	Positive power supply
4	4	V _{SS}	-	Negative power supply, ground
5~8	5~8	COM0~COM3	O	LCD COM outputs
9~47	-	SEG0~SEG38	-	LCD SEG outputs
48	-	V _{LCD} /SEG39	-	LCD drive voltage input/output Multiplexed pin with LCD SEG39 Pin function selectable via command
-	9~51	SEG0~SEG42	O	LCD SEG outputs
-	52	V _{LCD} /SEG43	-	LCD drive voltage input/output Multiplexed pin with LCD SEG43 Pin function selectable via command

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, All voltage referenced to V_{SS}, unless otherwise specified)

Characteristic	Symbol	Conditions	Value	Unit
supply voltage	-	-	V _{SS} -0.3 to V _{SS} +6.5	V
input voltage	V _{IN}	-	V _{SS} -0.3 to V _{DD} +0.3	V
operating temperature	T _{amb}	-	-40 to +85	℃
storage temperature	T _{stg}	-	-55 to +150	℃

3.2、Electrical Characteristics

3.2.1、DC Characteristics 1

(T_{amb}=-40 to +85℃, V_{DD}=2.4 to 5.5V, V_{SS}=0V, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
operating voltage	V _{DD}	-	-	2.4	-	5.5	V
operating voltage	V _{LCD}	-	-	-	-	V _{DD}	V
operating current	I _{DD}	3V	no load, V _{LCD} =V _{DD} , 1/3 bias, f _{LCD} =80Hz, LCD display on, internal system oscillator on, DA0~DA3 are set to "0000"	-	18	27	uA
		5V		-	25	40	uA
operating current	I _{DD1}	3V	no load, V _{LCD} =V _{DD} , 1/3 bias, f _{LCD} =80Hz, LCD display off, internal system oscillator on, DA0~DA3 are set to "0000"	-	2	5	uA
		5V		-	4	10	uA
standby current	I _{STB}	3V	no load, V _{LCD} =V _{DD} , LCD display off, internal system oscillator off	-	-	1	uA
		5V		-	-	2	uA



HIGH level input current	V_{IH}	-	SDA, SCL	$0.7V_{DD}$	-	V_{DD}	V
LOW level input current	V_{IL}	-	SDA, SCL	0	-	$0.3V_{DD}$	V
input leakage current	I_{IL}	-	$V_{IN}=V_{SS}$ or V_{DD}	-1	-	1	μA
LOW level output current	I_{OL}	3V	$V_{OL}=0.4V$, SDA	3	-	-	mA
		5V		6	-	-	mA
LCD COM sink current	I_{OL1}	3V	$V_{LCD}=3V$, $V_{OL}=0.3V$	250	400	-	μA
		5V	$V_{LCD}=5V$, $V_{OL}=0.5V$	500	800	-	μA
LCD COM source current	I_{OH1}	3V	$V_{LCD}=3V$, $V_{OH}=2.7V$	-140	-230	-	μA
		5V	$V_{LCD}=5V$, $V_{OH}=4.5V$	-300	-500	-	μA
LCD SEG sink current	I_{OL2}	3V	$V_{LCD}=3V$, $V_{OL}=0.3V$	250	400	-	μA
		5V	$V_{LCD}=5V$, $V_{OL}=0.5V$	500	800	-	μA
LCD SEG source current	I_{OH2}	3V	$V_{LCD}=3V$, $V_{OH}=2.7V$	-140	-230	-	μA
		5V	$V_{LCD}=5V$, $V_{OH}=4.5V$	-300	-500	-	μA

3.2.2、AC Characteristics 1

($T_{amb}=-40$ to $+85^{\circ}C$, $V_{DD}=2.4$ to $5.5V$, $V_{SS}=0V$, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
LCD frame frequency	f_{LCD1}	4V	1/4 duty, $T_{amb}=+25^{\circ}C$	-	80	-	Hz
LCD frame frequency	f_{LCD2}	4V	1/4 duty, $T_{amb}=-40$ to $+85^{\circ}C$	-	80	-	Hz
LCD frame frequency	f_{LCD3}	4V	1/4 duty, $T_{amb}=+25^{\circ}C$	-	160	-	Hz
LCD frame frequency	f_{LCD4}	4V	1/4 duty, $T_{amb}=-40$ to $+85^{\circ}C$	-	160	-	Hz
V_{DD} off time	t_{OFF}	-	V_{DD} drop down to 0V	20	-	-	ms
V_{DD} slew rate	t_{SR}	-	-	0.05	-	-	V/ms

Note:

1. During the power on/off period, if the conditions of the power-on reset sequence are not met, the internal power-on reset (POR) circuit cannot work normally.
2. During operating, if the V_{DD} voltage drops below the specified minimum operating voltage, the power-on reset sequence conditions must be satisfied. In other words, the V_{DD} voltage must drop to 0V and must maintain a 0V voltage of at least 20ms before rising to the normal operating voltage.

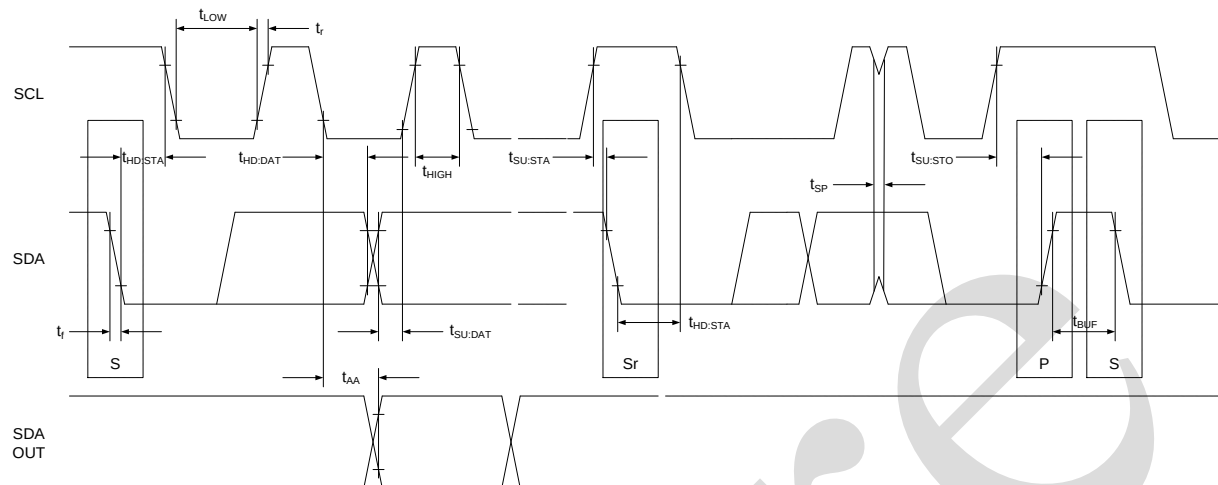


3.2.3、AC Characteristics 2 (I²C Interface)

Parameter	Symbol	Conditions	V _{DD} =2.4V to 5.5V		V _{DD} =3.0V to 5.5V		Unit
			Min.	Max.	Min.	Max.	
clock frequency	f _{SCL}	-	-	100	-	400	kHz
bus free time	t _{BUF}	during this period the bus must be free until a new transmission starts	4.7	-	1.3	-	us
Start condition hold time	t _{HD: STA}	after this period, the first clock pulse is generated	4.0	-	0.6	-	us
SCL LOW time	t _{LOW}	-	4.7	-	1.3	-	us
SCL HIGH time	t _{HIGH}	-	4.0	-	0.6	-	us
Start condition setup time	t _{SU: STA}	only relevant for repeated START condition	4.7	-	0.6	-	us
data hold time	t _{HD: DAT}	-	0	-	0	-	ns
data setup time	t _{SU: DAT}	-	250	-	100	-	ns
SDA and SCL rise time	t _R	-	-	1	-	0.3	us
SDA and SCL fall time	t _F	-	-	0.3	-	0.3	us
Stop condition setup time	t _{SU: STO}	-	4	-	0.6	-	us
effective clock output time	t _{AA}	-	-	3.5	-	0.9	us
input filter time constant (SDA, SCL)	t _{SP}	noise suppression time	-	100	-	50	ns

4、Timing Diagrams

4.1、I²C Timing



5、Precautions When Powering On

An internal reset circuit automatically initializes AiP16C22 when power is turned on.

Tips:

1. When the power is off, the power drop time is recommended to be $>1\text{ms}$
2. After the power is turned off, the voltage on the power supply is recommended to be $<0.1\text{V}$
3. It is recommended to keep the power off for $>100\text{ms}$ before powering it back on
4. When the power is powered on, it is recommended that the power rise time be $>1\text{ms}$

When the power is applied, the device is initialized by an internal power-on reset circuit. The status of the internal circuits after initialization is as follows:

Function	Reset status
LCD display	OFF
System oscillator	OFF
Blinking function	OFF
LCD bias generator	OFF
VLCD adjustment function	OFF
VLCD pin	VLCD output disable
COM/SEG output	VLCD
Frame frequency	80Hz
Duty	1/4 duty
VLCD bias	1/3 bias



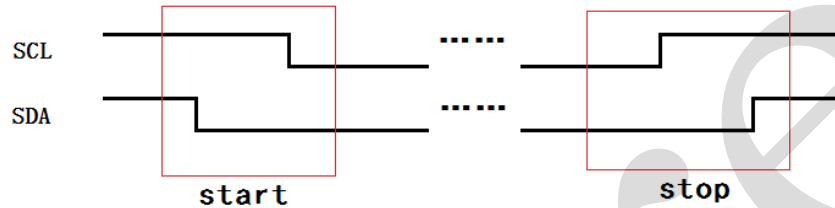
6、Function Description

6.1、I²C Interface

The chip provides a standard I²C serial interface that include two PADs, a serial data line SDA and a serial clock line SCL. Each of these lines is connected to the positive power supply via a pull-up resistor with a typical value of 4.7KΩ. Both lines are high when the I²C bus is idle. The microcontroller connected to the I²C interface must have an open drain output to achieve wired-or function.

6.2、Data Validity

The start and stop signs of the clock signal are detected at high power level:

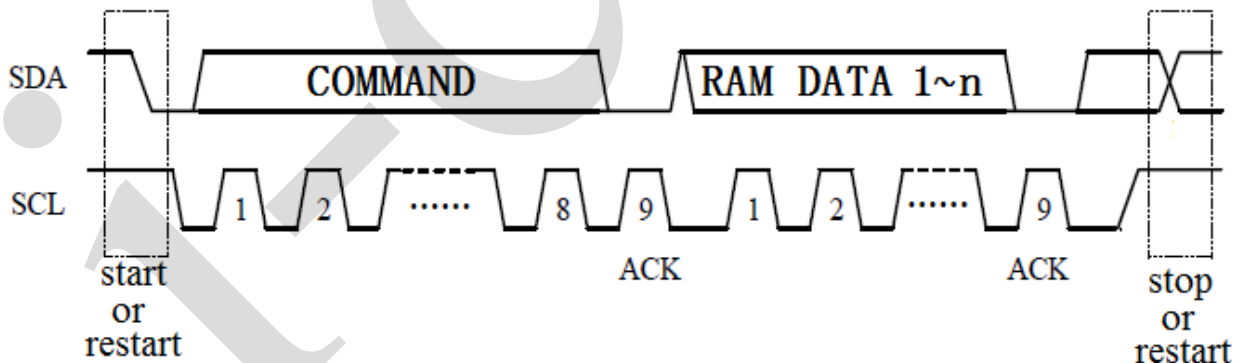


Therefore, in the data transmission phase, during SCL=1, the data bit of the SDA pin must remain stable, and only when SCL=0, the level of the SDA pin is allowed to change. Otherwise, an incorrect start or stop flag will be detected, resulting in transmission interruption.

The chip can detect the restart (repeat start) flag by typing the START flag again at any moment before the stop flag. Restart stops the current communication cycle directly, while restarting a new communication cycle.

6.3、Byte Format

Refer to the standard I²C format for 8 data clocks and 1 answer clock per communication cycle. The sender sends 8 bits of data each time, after which the receiver sends 1bit of low level answer signal (ACK) in the ninth, informing the sender that the data is sent and can continue to send data.



In the reply phase, the data receiver may also send a 1bit high level No answer signal (NACK) to inform the sender of the end of the data transmission. In this case, the host should generate either a stop signal or a restart signal.



6.4、Slave Address

Referring to the standard I²C format, after the host sends the START signal, it first sends the slave address bytes to match the slave. The AiP16C22 address bit is "0111111".

The addressing byte 8bit of data is the read/write control bit (R/W), which is used to indicate whether the subsequent operation is a read or write operation. R/W is 1 for subsequent read operations, and R/W is 0 for subsequent write operations.

MSB								LSB	
0	1	1	1	1	1	1	1	R/W	

7、Command Set

No.	Function	MSB-----LSB								Description
		B7	B6	B5	B4	B3	B2	B1	B0	
1	Mode setting	1	0	0	F	E1	E0	0	B	Reset value: 0x80
2	Address pointer	0	0	0	A4	A3	A2	A1	A0	Reset value: 0x00
3	Blink frequency	1	1	0	0	0	0	B1	B0	Reset value: 0xC0
4	Internal voltage adjustment setting	0	1	S1	S0	DA3	DA2	DA1	DA0	Reset value: 0x70

7.1、Command Description

No.	Function	MSB-----LSB								Description
		B7	B6	B5	B4	B3	B2	B1	B0	
1	Mode setting	1	0	0	F	E1	E0	0	B	Reset value: 0x80
	F	Reset value: 0 =0, frame rate 80Hz =1, frame rate 160Hz								
	E1, E0	Reset value: 00 =0X, internal clock off, display off =10, internal clock on, display off =11, internal clock on, display on								
	B	Reset value: 0 =0, 1/3 bias =1, 1/2 bias								



No.	Function	MSB-----LSB								Description
		B7	B6	B5	B4	B3	B2	B1	B0	
2	Address pointer	0	0	0	A4	A3	A2	A1	A0	Reset value: 0x00
A4~A0		Reset value: 00000 Memory-mapped start address of display data, configurable range: 00000~10101 During read/write operations to the memory, the memory address is automatically incremented by 1 after the operation is completed. If the address reaches 15H, the pointer resets to 00H								

No.	Function	MSB-----LSB								Description
		B7	B6	B5	B4	B3	B2	B1	B0	
3	Blink frequency	1	1	0	0	0	0	B1	B0	Reset value: 0xC0
B1, B0		Reset value: 00 =00, blink off =01, blink on, 2Hz =10, blink on, 1Hz =11, blink on, 0.5Hz								

No.	Function	MSB-----LSB								Description
		B7	B6	B5	B4	B3	B2	B1	B0	
4	Internal voltage adjustment setting	0	1	S1	S0	DA3	DA2	DA1	DA0	Reset value: 0x70
S1, S0		Reset value: 00 =00, VLCD/SEG39 pin configured as VLCD, VLCD voltage is input through the VLCD pin =01, VLCD/SEG39 pin configured as VLCD, VLCD voltage is generated internally and controlled by DA bit =10, VLCD/SEG39 pin configured as SEG39, VLCD voltage equals the power supply (VDD) voltage =11, VLCD/SEG39 pin configured as SEG39, VLCD voltage is generated internally and controlled by DA bit								
DA[3:0]		Reset value: 0000 Used to adjust VLCD when S=01 or 11 =0000, VLCD voltage highest, VLCD voltage follower off =1111, VLCD voltage lowest, VLCD voltage follower on See the VLCD Voltage Adjustment section for specific information								



8、Display RAM

AiP16C22 has static RAM for storing LCD display data. Write "1" to it and the corresponding LCD will light up, write "0" and the corresponding LCD will dim.

The RAM data content is mapped directly to the LCD. The SEGs in column 1 of RAM work with its corresponding COM0. In complex LCD applications, the SEGs in columns 2, 3, and 4 are time-multiplexed with their COM1, COM2, and COM3 counterparts, respectively. RAM data is mapped to LCD mode as follows:

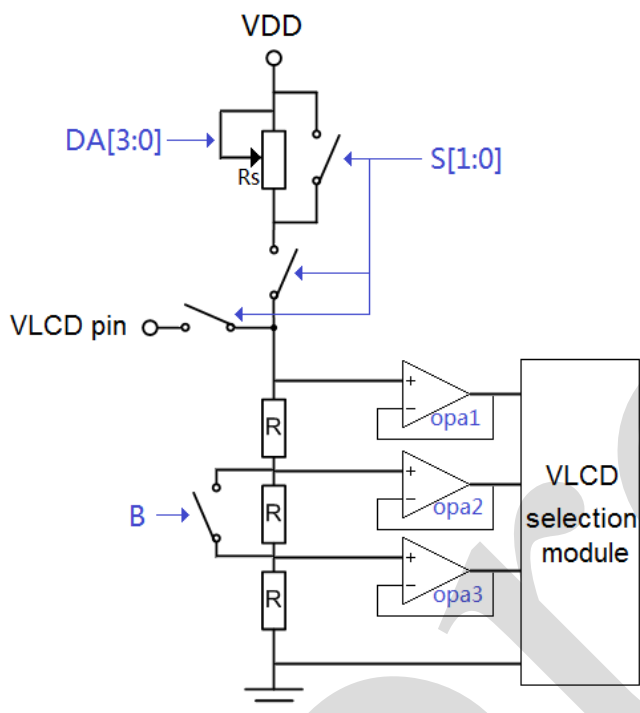
RAM Address	Display point							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	C3×S1	C2×S1	C1×S1	C0×S1	C3×S0	C2×S0	C1×S0	C0×S0
01H	C3×S3	C2×S3	C1×S3	C0×S3	C3×S2	C2×S2	C1×S2	C0×S2
02H	C3×S5	C2×S5	C1×S5	C0×S5	C3×S4	C2×S4	C1×S4	C0×S4
03H	C3×S7	C2×S7	C1×S7	C0×S7	C3×S6	C2×S6	C1×S6	C0×S6
04H	C3×S9	C2×S9	C1×S9	C0×S9	C3×S8	C2×S8	C1×S8	C0×S8
05H	C3×S11	C2×S11	C1×S11	C0×S11	C3×S10	C2×S10	C1×S10	C0×S10
06H	C3×S13	C2×S13	C1×S13	C0×S13	C3×S12	C2×S12	C1×S12	C0×S12
07H	C3×S15	C2×S15	C1×S15	C0×S15	C3×S14	C2×S14	C1×S14	C0×S14
08H	C3×S17	C2×S17	C1×S17	C0×S17	C3×S16	C2×S16	C1×S16	C0×S16
09H	C3×S19	C2×S19	C1×S19	C0×S19	C3×S18	C2×S18	C1×S18	C0×S18
.....								
14H	C3×S41	C2×S41	C1×S41	C0×S41	C3×S40	C2×S40	C1×S40	C0×S40
15H	C3×S43	C2×S43	C1×S43	C0×S43	C3×S42	C2×S42	C1×S42	C0×S42

Note:

Cn x Sn indicates the pixel points controlled by COMn and SEGn.



9、VLCD Generator



- The relationship between 4-bit programmable analog switch and V_{LCD} output voltage is shown in the following table:

Bias DA3~DA0	1/3	1/2	Description
00H	$1.000 \times V_{DD}$	$1.000 \times V_{DD}$	Reset value
01H	$0.944 \times V_{DD}$	$0.9375 \times V_{DD}$	
02H	$0.894 \times V_{DD}$	$0.882 \times V_{DD}$	
03H	$0.849 \times V_{DD}$	$0.833 \times V_{DD}$	
04H	$0.808 \times V_{DD}$	$0.789 \times V_{DD}$	
05H	$0.771 \times V_{DD}$	$0.750 \times V_{DD}$	
06H	$0.738 \times V_{DD}$	$0.714 \times V_{DD}$	
07H	$0.707 \times V_{DD}$	$0.682 \times V_{DD}$	
08H	$0.678 \times V_{DD}$	$0.652 \times V_{DD}$	
09H	$0.652 \times V_{DD}$	$0.652 \times V_{DD}$	
0AH	$0.628 \times V_{DD}$	$0.600 \times V_{DD}$	
0BH	$0.605 \times V_{DD}$	$0.577 \times V_{DD}$	
0CH	$0.584 \times V_{DD}$	$0.556 \times V_{DD}$	
0DH	$0.565 \times V_{DD}$	$0.536 \times V_{DD}$	
0EH	$0.547 \times V_{DD}$	$0.517 \times V_{DD}$	
0FH	$0.529 \times V_{DD}$	$0.500 \times V_{DD}$	



10、SEG Drive Output

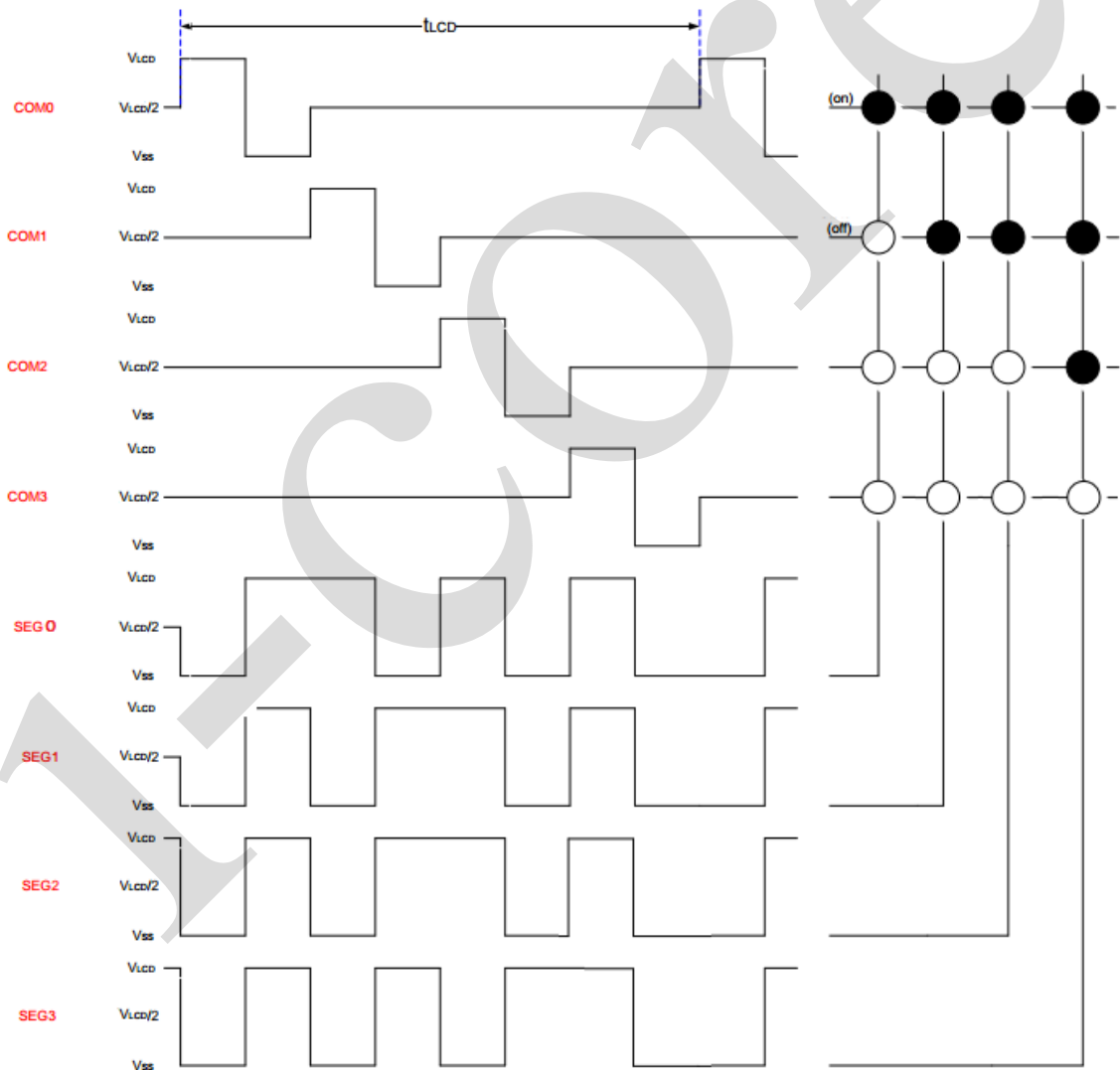
SEG should be directly connected to the LCD panel. Generate SEG output signals based on the multiplexed COM signal and the data inside the display latch, and the unused SEG output should remain open.

11、COM Drive Output

COM should be directly connected to the LCD panel. Generate a COM output signal according to the selected LCD driver mode, and the unused COM output should remain open.

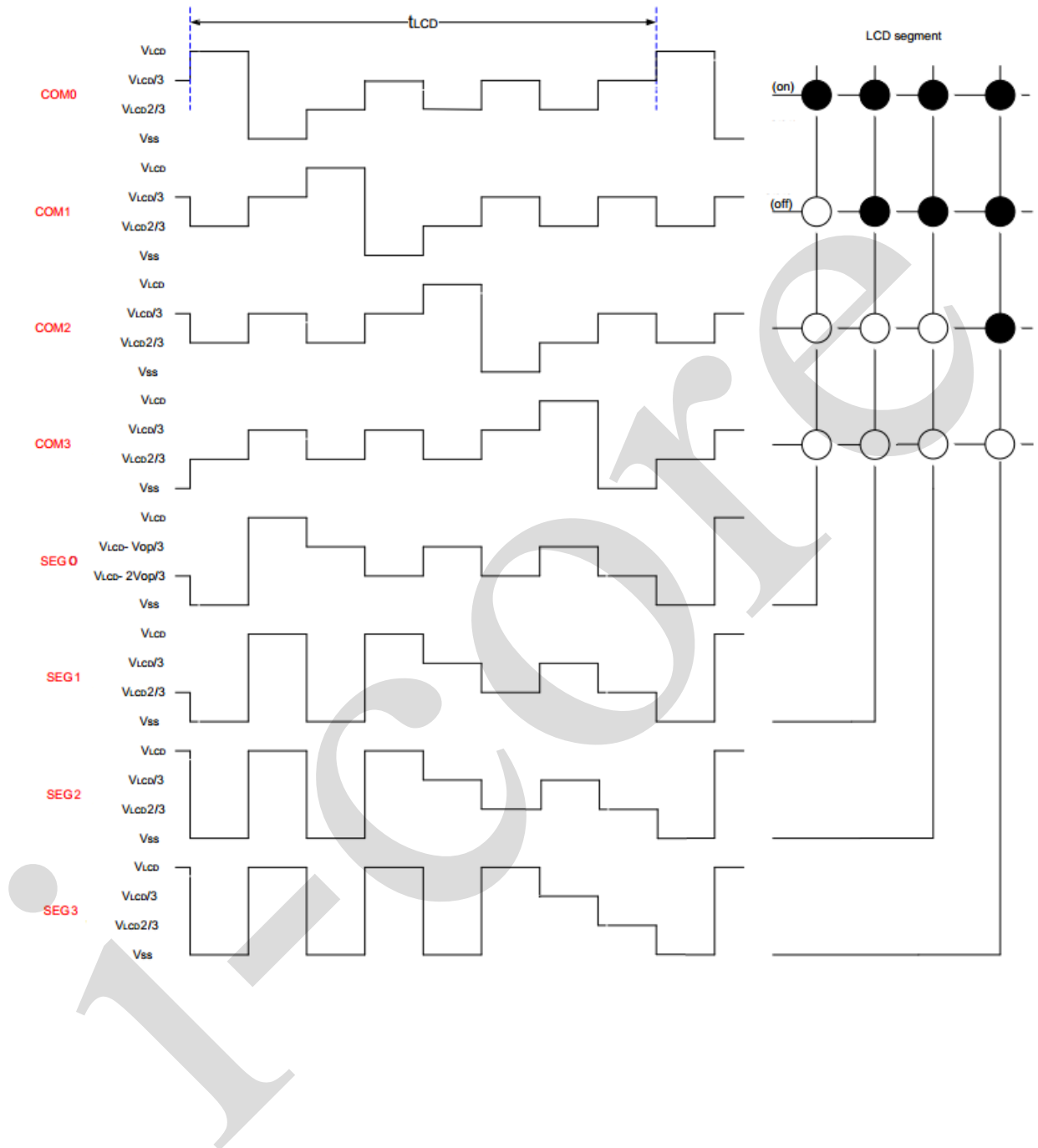
12、LCD Driver Mode Waveform

When the LCD driver mode is selected 1/2 bias, its waveform and LCD display are as shown in the following figure:





When the LCD driver mode is selected 1/3 bias, its waveform and LCD display are as shown in the image below:





13、Recommend Workflow**13.1、Initialization**

1. Power-on
2. Delay until the power supply is stable
3. Set VLCD bias and duty cycle
4. Set the frame rate
5. Set the VLCD/SEG shared pin function
6. Set the flicker function

13.2、Display Data Read/Write (Address Setting)

1. Set the RAM address
2. Read/write RAM data
3. Turn on the internal clock and display

13.3、Power Supply Sequence

If the VLCD and VDD pins are powered separately, it is highly recommended to follow the power supply sequence requirements:

1. Power on VDD first when starting, and then power on VLCD after VDD stabilizes
2. Shutdown VLCD first power off, VLCD reduced to 0.3V below, and then make VDD power off

If the startup process violates the above power supply voltage supply sequence, it may cause initialization errors.

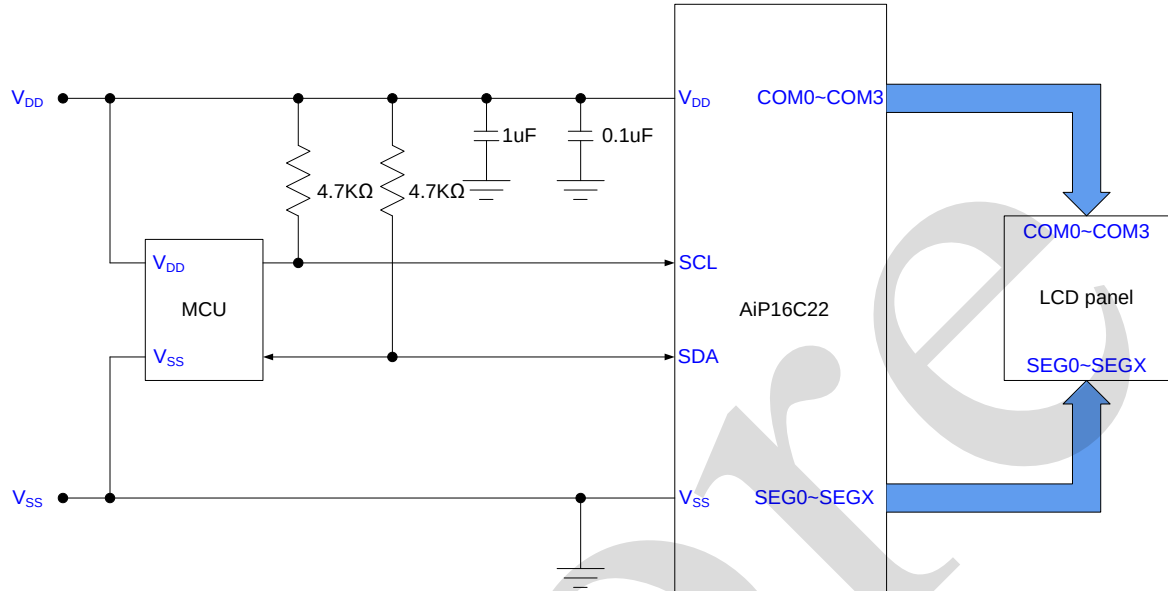
If the shutdown process violates the above power supply voltage supply sequence, it may cause confusion during the power failure process.



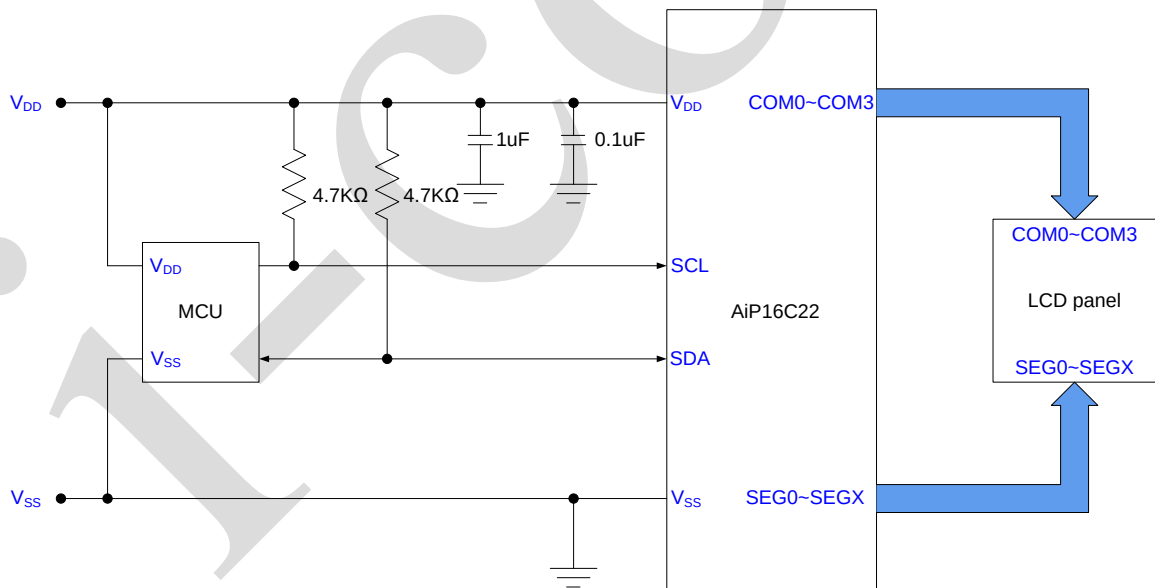
14、Typical Application Lines and Instructions

14.1、When SEG/VLCD Pin Configured As SEG Pin

The internal voltage adjustment function is disabled, and the bias voltage is supplied by the internal V_{DD} power supply.



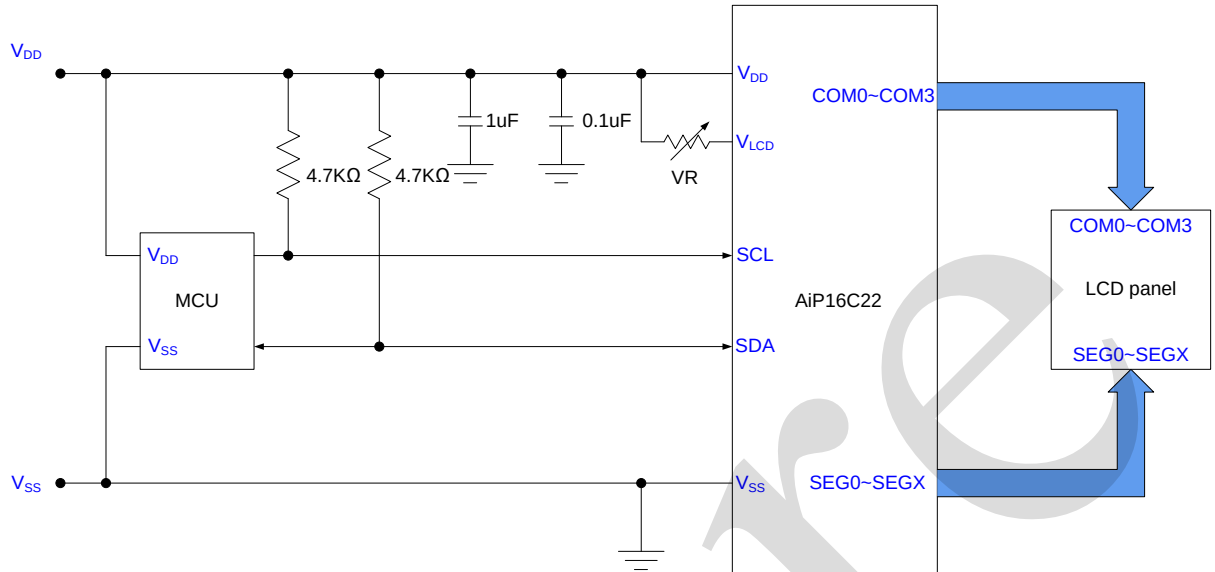
The internal voltage adjustment function is enabled, and the bias voltage is supplied by the internal adjustment module.



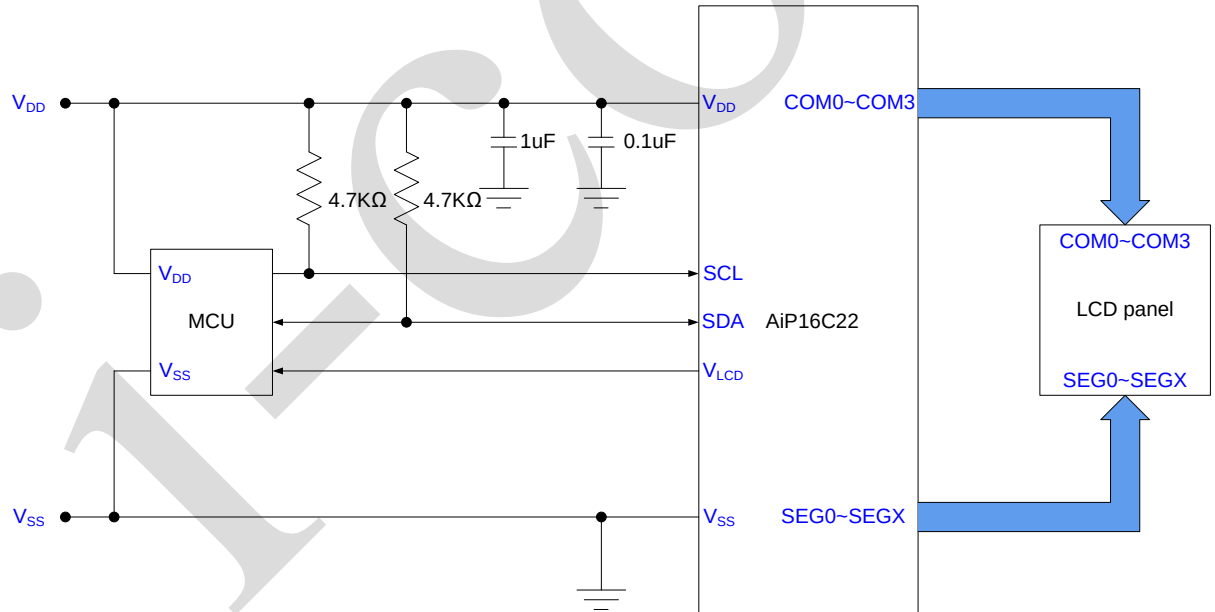


14.2、When SEG/VLCD Pin Configured As V_{LCD} Pin

The internal voltage adjustment function is disabled, and an external resistor must be connected between the V_{LCD} and V_{DD} pins to adjust the bias voltage.



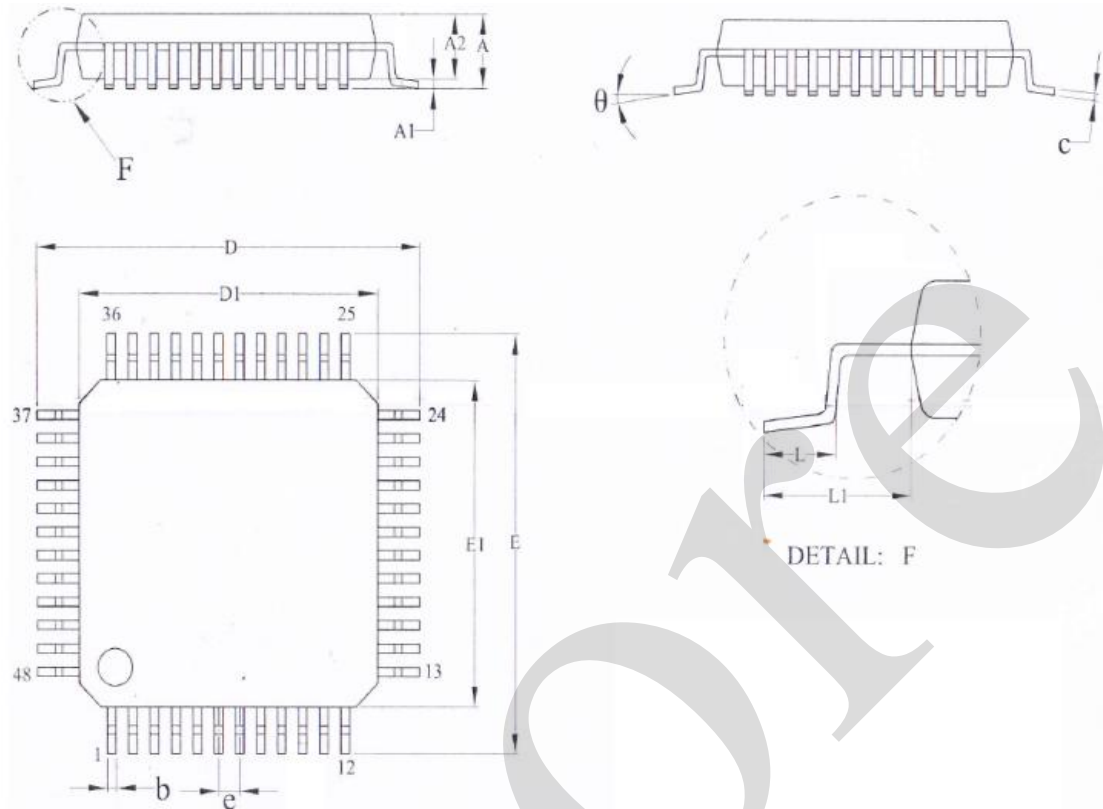
The internal voltage adjustment function is enabled, and the V_{LCD} pin voltage can be detected by connecting it to the MCU.





15、Package Information

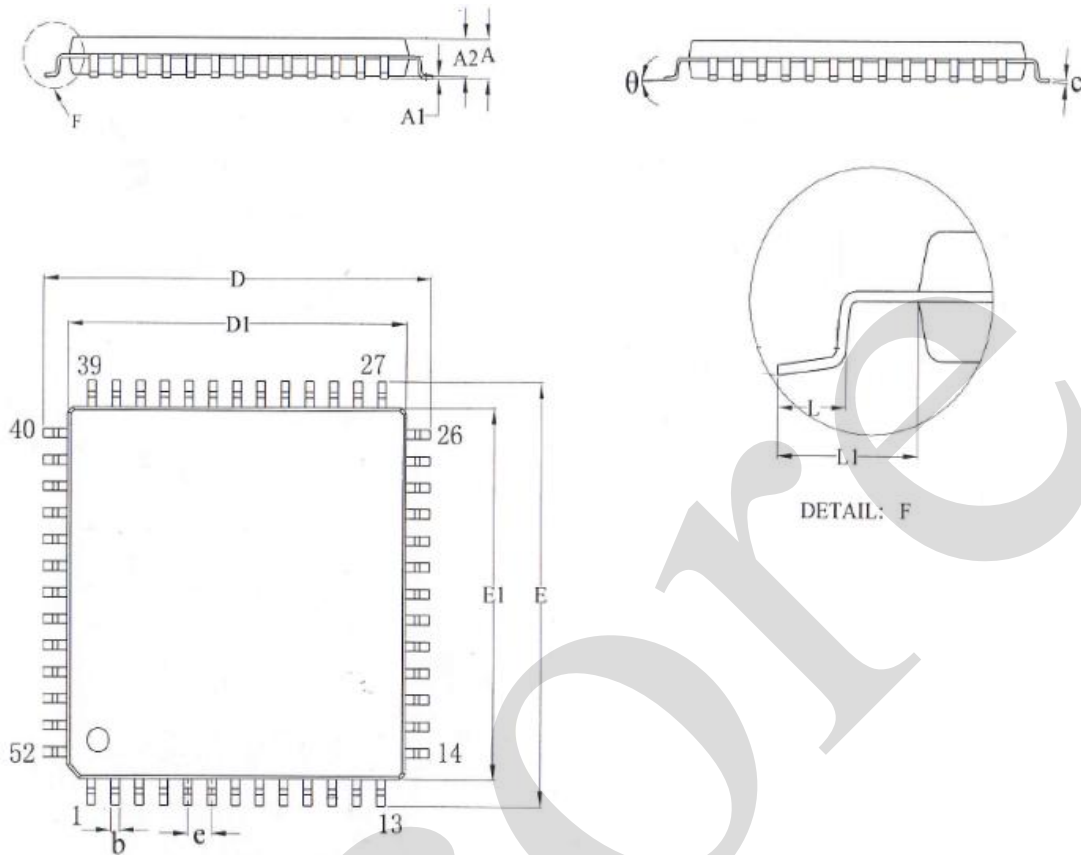
15.1、LQFP48



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	1.45	1.65
A1	0.05	0.20
A2	1.30	1.50
b	0.17	0.27
c	0.09	0.20
D	8.80	9.20
D1	6.90	7.10
E	8.80	9.20
E1	6.90	7.10
e	0.50	
L	0.43	0.80
L1	1.00	
θ	0°	10°



15.2、LQFP52



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	—	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.38	0.46
c	0.13	0.17
D	15.80	16.20
D1	13.90	14.10
E	15.80	16.20
E1	13.90	14.10
e	1.00	
L	0.45	0.75
L1	1.00	
θ	0°	7°



16、Statements And Notes

16.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

16.2、Notes

We recommend you to read this chapter carefully before using this product.

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