



AiP1944

3-line Serial Interface/Common Cathode

16Seg 16Grid or 24Seg 8Grid LED

Controller/Driver with 16*2

Keyboard Scan Ports

Product Specification

Specification Revision History:

Version	Data	Description
2018-11-A1	2018-11	New
2019-04-A2	2019-04	Replace the new template
2019-07-A3	2019-07	Add Ordering Information
2021-12-A4	2021-12	Modify Ordering Information



1、General Description

AiP1944 is an LED Controller, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer.

Features:

- Multiple display modes
- 16SEG*16GRID~24SEG*8GRID display mode
- 16*2 Key scanning
- 8-step dimming circuitry
- Serial interface (CLK, STB, DIO)
- Built-in RC oscillator
- Package: LQFP44

Applications:

Multi-pen LED display panel, for example: the electromobile display panel.

Order information:

Tube packing specifications:

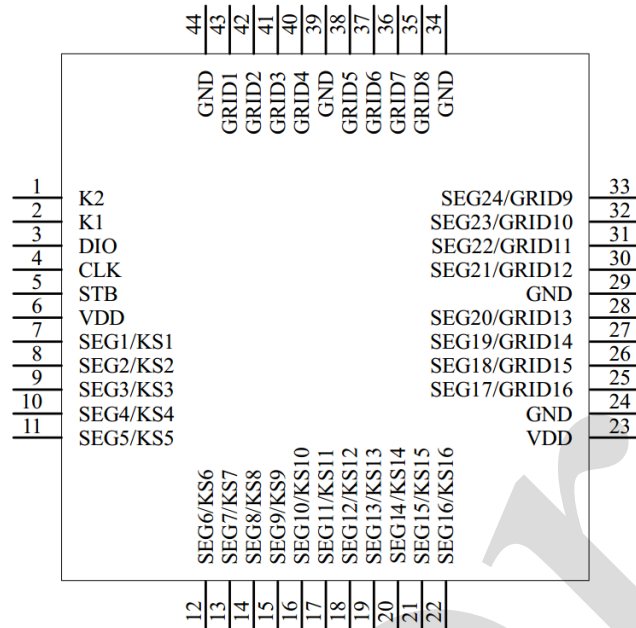
Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP1944LB44.TB	LQFP44	AiP1944	160 PCS/plate	10 plate/box	1600 PCS/box	Dimensions of plastic enclosure: 10mm×10mm Pin spacing: 0.8mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



2、Block Diagram And Pin Description

2.1、Pin Configurations



2.2、Pin Description

Pin No.	Pin Name	I/O	Description
1	K2	I	Key input port, buit in pull-down resistance
2	K1	I	Key input port, buit in pull-down resistance
3	DIO	IO	Data Pin, N-Channel Open-Drain, buit in pull-up resistance
4	CLK	I	Clock Pin, buit in pull-up resistance
5	STB	I	Serial Interface Strobe Pin, buit in pull-up resistance
6,23	VDD	-	Power
7	SEG1/KS1	O	SEG output/Keystroke output, N-Channel Open-Drain
8	SEG2/KS2	O	SEG output/Keystroke output, N-Channel Open-Drain
9	SEG3/KS3	O	SEG output/Keystroke output, N-Channel Open-Drain
10	SEG4/KS4	O	SEG output/Keystroke output, N-Channel Open-Drain
11	SEG5/KS5	O	SEG output/Keystroke output, N-Channel Open-Drain
12	SEG6/KS6	O	SEG output/Keystroke output, N-Channel Open-Drain
13	SEG7/KS7	O	SEG output/Keystroke output, N-Channel Open-Drain
14	SEG8/KS8	O	SEG output/Keystroke output, N-Channel Open-Drain
15	SEG9/KS9	O	SEG output/Keystroke output, N-Channel Open-Drain
16	SEG10/KS10	O	SEG output/Keystroke output, N-Channel Open-Drain
17	SEG11/KS11	O	SEG output/Keystroke output, N-Channel Open-Drain
18	SEG12/KS12	O	SEG output/Keystroke output, N-Channel Open-Drain



19	SEG13/KS13	O	SEG output/Keystroke output, N-Channel Open-Drain
20	SEG14/KS14	O	SEG output/Keystroke output, N-Channel Open-Drain
21	SEG15/KS15	O	SEG output/Keystroke output, N-Channel Open-Drain
22	SEG16/KS16	O	SEG output/Keystroke output, N-Channel Open-Drain
24,29,34,39,44	GND	-	GND
25	SEG17/GRID16	O	SEG/GRID multiplexing output, N/P-Channel Open-Drain
26	SEG18/GRID15	O	SEG/GRID multiplexing output, N/P-Channel Open-Drain
27	SEG19/GRID14	O	SEG/GRID multiplexing output, N/P-Channel Open-Drain
28	SEG20/GRID13	O	SEG/GRID multiplexing output, N/P-Channel Open-Drain
30	SEG21/GRID12	O	SEG/GRID multiplexing output, N/P-Channel Open-Drain
31	SEG22/GRID11	O	SEG/GRID multiplexing output, N/P-Channel Open-Drain
32	SEG23/GRID10	O	SEG/GRID multiplexing output, N/P-Channel Open-Drain
33	SEG24/GRID9	O	SEG/GRID multiplexing output, N/P-Channel Open-Drain
35	GRID8	O	GRID output, P-Channel Open-Drain
36	GRID7	O	GRID output, P-Channel Open-Drain
37	GRID6	O	GRID output, P-Channel Open-Drain
38	GRID5	O	GRID output, P-Channel Open-Drain
40	GRID4	O	GRID output, P-Channel Open-Drain
41	GRID3	O	GRID output, P-Channel Open-Drain
42	GRID2	O	GRID output, P-Channel Open-Drain
43	GRID1	O	GRID output, P-Channel Open-Drain

3、Electrical Parameter

3.1、Absolute Maximum Ratings

($T_{amb}=25^{\circ}\text{C}$, GND=0V, unless otherwise specified.)

Parameter	Symbol	Conditions	Value	Unit
Power Supply Voltage	VDD	-	-0.5~+7.0	V
Input Voltage	V_{IN}	-	-0.5~VDD+0.5	V
Drive output current	I_{O1}	SEG	-50	mA
	I_{O2}	GRID	+150	mA
Operating Temperature	T_{opt}	-	-40~+85	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-	-65~+150	$^{\circ}\text{C}$
Soldering Temperature	T_L	10s	250	$^{\circ}\text{C}$



3.2、Recommended Operating Range

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	VDD	3	5	5.5	V
Input high-level voltage	V _{IH}	0.7VDD	-	VDD	V
Input low-level voltage	V _{IL}	0	-	0.2VDD	V

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(VDD=5V, GND=0V, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output high-level driver	I _{OH1}	V _O =VDD-2V, SEGn	-20	-25	-40	mA
	I _{OH2}	V _O =VDD-3V, SEGn	-20	-30	-50	mA
Output low-level driver	I _{OL1}	V _O =0.3V, GRIDn	80	100	-	mA
	I _{DO}	V _O =0.4V, DIO	4	8	-	mA
High-level output current tolerance	I _{TOLSG}	V _O =VDD-3V, SEGn	-	-	5	%
Input high-level voltage	V _{IH}	CLK, DIO, STB	0.7VDD	-	-	V
Input low-level voltage	V _{IL}	CLK, DIO, STB	-	-	0.2VDD	V
Hysteresis Voltage	V _H	CLK, DIO, STB	-	0.35	-	V
Input leakage current	I _I	V _{IN} =VDD CLK,DIO,STB	-	-	±1	uA
		V _{IN} =GND CLK,DIO,STB	300	500	700	uA
Static current	I _{DD}	No load, V _{IN} =VDD	200	220	250	uA
Input pull-up resistance	R _H	CLK、DIO、STB	-	10	-	KΩ
Input pull-down resistance	R _L	K1~K2	-	5	-	KΩ

3.3.2、AC Characteristics 1

(VDD=4.5~5.5V, GND=0V, unless otherwise specified.)

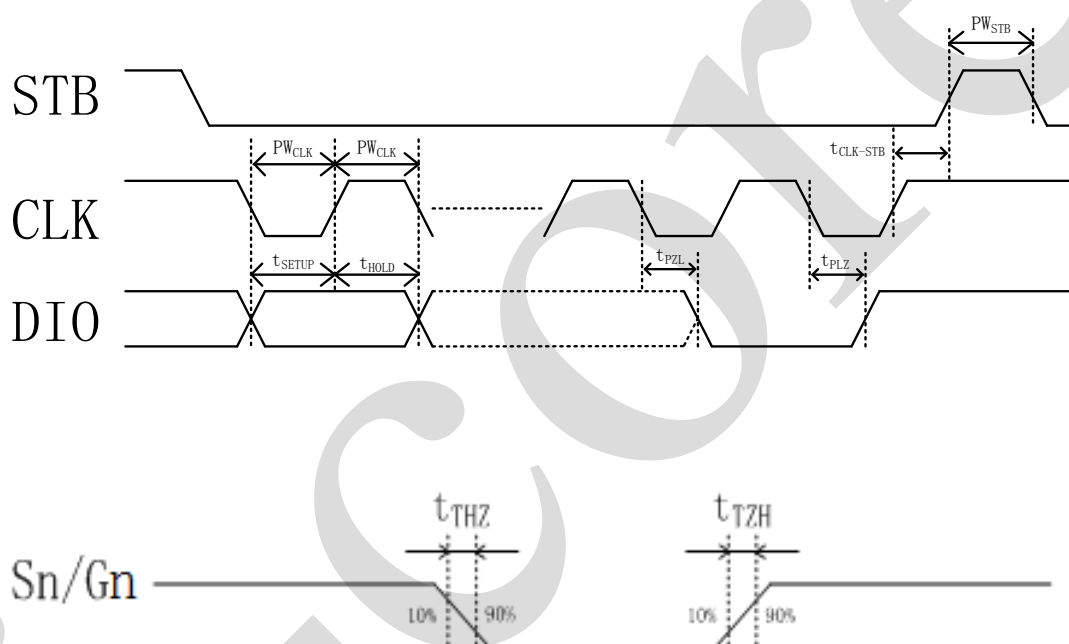
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	f _{OSC}	-	-	400	-	KHz
Propagation delay	t _{PLZ}	CLK→DIO C _L =15pF, R _L =10KΩ	-	-	300	ns
	t _{PZL}		-	-	100	ns
Rise time	t _{TZH1}	C _L =300pF	SEGn		2	us
	t _{TZH}		GRIDn		0.5	us
Fall time	t _{THZ}	C _L =300pF SEGn, GRIDn	-	-	120	us
Maximum clock frequency	f _{max}	Duty=50%	1	-	-	MHz



3.3.3、AC Characteristics 2

(VDD=4.5~5.5V, GND=0V, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse width	PW_{CLK}	-	400	-	-	ns
STB pulse width	PW_{STB}	-	1	-	-	us
Set-up time for data	t_{SETUP}	-	100	-	-	ns
Hold time for data	t_{HOLD}	-	100	-	-	ns
CLK→STB time	$t_{CLK\ STB}$	CLK↑→STB↑	1	-	-	us
Wait time	t_{WAIT}	CLK↑→CLK↓	1	-	-	us





4、Function Description

4.1、Display Register Address

This register stores data transmitted from external devices to AiP1944 through serial interface. When writing LED display data, it displays low address to high level according to the display address, and from the low to high operation of data byte, the address is allocated as follows:

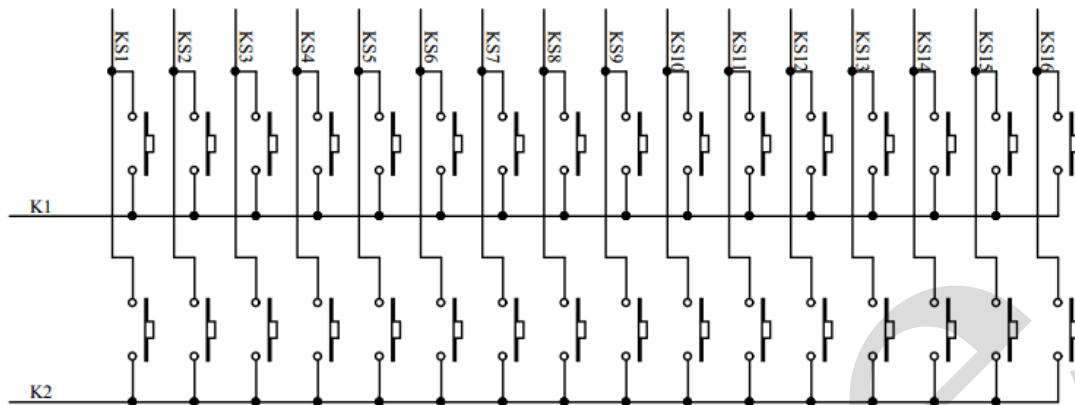
Invalid data																																			
SEG24	SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	B0	B1	B2	B3	B4	B5	B6	B7				
00H								01H								02H								03H								GRID1			
04H								05H								06H								07H								GRID2			
08H								09H								0AH								0BH								GRID3			
0CH								0DH								0EH								0FH								GRID4			
10H								11H								12H								13H								GRID5			
14H								15H								16H								17H								GRID6			
18H								19H								1AH								1BH								GRID7			
1CH								1DH								1EH								1FH								GRID8			
20H								21H								22H								23H								GRID9			
24H								25H								26H								27H								GRID10			
28H								29H								2AH								2BH								GRID11			
2CH								2DH								2EH								2FH								GRID12			
30H								31H								32H								33H								GRID13			
34H								35H								36H								37H								GRID14			
38H								39H								3AH								3BH								GRID15			
3CH								3DH								3EH								3FH								GRID16			

Note: When power up, first transfer data to RAM, and then setup display on.



4.2、Key Scan And Key Sweep Data Register

The bond sweep matrix is 16*2, as shown below:



Key scan data storage address is shown as follows, first read key command, start reading key data BYTE1 - BYTE4 bytes, read data from the low start output. When the key of the chip K and the KS pin is pressed, the Bit bit in the corresponding byte is 1.

B0	B1	B2	B3	B4	B5	B6	B7	
K1	K2	K1	K2	K1	K2	K1	K2	
KS1		KS2		KS3		KS4		BYTE1
KS5		KS6		KS7		KS8		BYTE2
KS9		KS10		KS11		KS12		BYTE3
KS13		KS14		KS15		KS16		BYTE4

Note:

1. AiP1944 can read a maximum of 4 bytes, not allowed to read more.
2. Read data byte can read sequentially from the BYTE1 to BYTE4, do not cross byte read. For example: on the hardware K2 and KS10 corresponding button is pressed, the key is to read data, read the 4bit must be third bytes, can read data; when there are multiple key presses, such as K1 and KS10, K2 and KS10, press the two keys at the same time, BYTE3 bytes of B2 B3 is 1.
3. The combination key can only be the same KS, different K combinations.



4.3、Commands Description

Each time the STB port is reduced by the height, the first byte of the circuit is sent from the DIO port to the instruction input, and the second byte acts as the data input. Two high bits in the instruction are used to distinguish different instructions.

B7	B6	Command
0	0	Display mode setting
0	1	Data command setting
1	0	Display control command setting
1	1	Address command setting

If STB is set to high level during instruction or data transmission, serial communication is initialized, and the instructions or data being transmitted are invalid.

4.3.1、Display Mode Setting

This instruction is used to set the number of selected drive segments and bits. When the instruction is executed, the display is forced to close. To redisplay, the opening/closing instruction “ON” must be executed, but when the same pattern is set, the above situation does not occur.

MSB		LSB						Display mode
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	Irrelevant item write 0		0	0	0	0	8 GRID 24 SEG
0	0			0	0	0	1	9 GRID 23 SEG
0	0			0	0	1	0	10 GRID 22 SEG
0	0			0	0	1	1	11 GRID 21 SEG
0	0			0	1	0	0	12 GRID 20 SEG
0	0			0	1	0	1	13 GRID 19 SEG
0	0			0	1	1	0	14 GRID 18 SEG
0	0			0	1	1	1	15 GRID 17 SEG
0	0			1	X	X	X	16 GRID 16 SEG

4.3.2、Data Command Setting

This instruction is used to set up data write and read, and B1 and B0 are not allowed to be set to 01 or 11.

MSB				LSB				Function	Instruction
B7	B6	B5	B4	B3	B2	B1	B0		
0	1	Irrelevant item write 0		-	-	0	0	Read / write mode setting	Write the data to the display register
0	1			-	-	1	0		Reading key keys
0	1			-	0	-	-	Address mode setting	Address self add mode
0	1			-	1	-	-		Fixed address mode
0	1			0	-	-	-	Test pattern setting	Normal mode
0	1			1	-	-	-		Test mode (Internal use)



4.3.3. Address Command Setting

This instruction is used to set up the address of the display register. If the address is set to 40H or higher, the data is ignored until the valid address is set. When the power is on, the address is set to 00H by default.

MSB				LSB				Display address
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	0	0	0	0	0	0	00H
1	1	0	0	0	0	0	1	01H
1	1	0	0	0	0	1	0	02H
1	1	0	0	0	0	1	1	03H
1	1	0	0	0	1	0	0	04H
1	1	0	0	0	1	0	1	05H
1	1	0	0	0	1	1	0	06H
1	1	0	0	0	1	1	1	07H
1	1	0	0	1	0	0	0	08H
1	1	0	0	1	0	0	1	09H
1	1	0	0	1	0	1	0	0AH
1	1	0	0	1	0	1	1	0BH
1	1	0	0	1	1	0	0	0CH
1	1	0	0	1	1	0	1	0DH
1	1	0	0	1	1	1	0	0EH
1	1	0	0	1	1	1	1	0FH
1	1	0	1	0	0	0	0	10H
1	1	0	1	0	0	0	1	11H
1	1	0	1	0	0	1	0	12H
1	1	0	1	0	0	1	1	13H
1	1	0	1	0	1	0	0	14H
1	1	0	1	0	1	0	1	15H
1	1	0	1	0	1	1	0	16H
1	1	0	1	0	1	1	1	17H
1	1	0	1	1	0	0	0	18H
1	1	0	1	1	0	0	1	19H
1	1	0	1	1	0	1	0	1AH
1	1	0	1	1	0	1	1	1BH
1	1	0	1	1	1	0	0	1CH
1	1	0	1	1	1	0	1	1DH
1	1	0	1	1	1	1	0	1EH
1	1	0	1	1	1	1	1	1FH
1	1	1	0	0	0	0	0	20H



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1	1	1	0	0	0	0	1	21H
1	1	1	0	0	0	1	0	22H
1	1	1	0	0	0	1	1	23H
1	1	1	0	0	1	0	0	24H
1	1	1	0	0	1	0	1	25H
1	1	1	0	0	1	1	0	26H
1	1	1	0	0	1	1	1	27H
1	1	1	0	1	0	0	0	28H
1	1	1	0	1	0	0	1	29H
1	1	1	0	1	0	1	0	2AH
1	1	1	0	1	0	1	1	2BH
1	1	1	0	1	1	0	0	2CH
1	1	1	0	1	1	0	1	2DH
1	1	1	0	1	1	1	0	2EH
1	1	1	0	1	1	1	1	2FH
1	1	1	1	0	0	0	0	30H
1	1	1	1	0	0	0	1	31H
1	1	1	1	0	0	1	0	32H
1	1	1	1	0	0	1	1	33H
1	1	1	1	0	1	0	0	34H
1	1	1	1	0	1	0	1	35H
1	1	1	1	0	1	1	0	36H
1	1	1	1	0	1	1	1	37H
1	1	1	1	1	0	0	0	38H
1	1	1	1	1	0	0	1	39H
1	1	1	1	1	0	1	0	3AH
1	1	1	1	1	0	1	1	3BH
1	1	1	1	1	1	0	0	3CH
1	1	1	1	1	1	0	1	3DH
1	1	1	1	1	1	1	0	3EH
1	1	1	1	1	1	1	1	3FH



4.3.4、Display Control Command Setting

The instruction is used to set the switch of the display and to adjust the brightness of the display. The circuit has a total of 8 levels of brightness for adjustment.

MSB

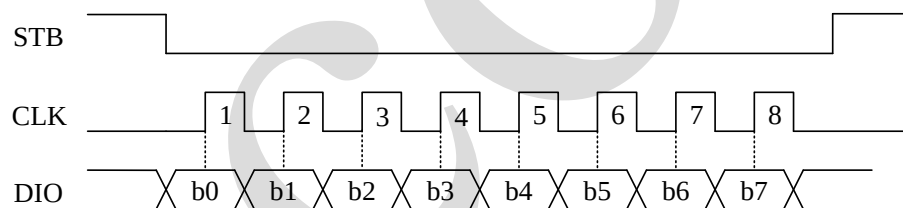
LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Instruction
1	0	Irrelevant item write 0		-	0	0	0	Display luminance setting	Pulse width = 1/16
1	0			-	0	0	1		Pulse width = 2/16
1	0			-	0	1	0		Pulse width = 4/16
1	0			-	0	1	1		Pulse width = 10/16
1	0			-	1	0	0		Pulse width = 11/16
1	0			-	1	0	1		Pulse width = 12/16
1	0			-	1	1	0		Pulse width = 13/16
1	0			-	1	1	1		Pulse width = 14/16
1	0			0	-	-	-	Display switch setting	Display off
1	0			1	-	-	-		Display on

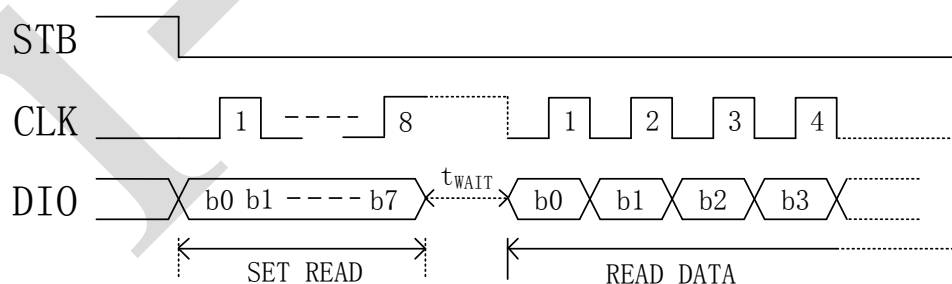
4.4、Serial Data Transmission Format

Reading and receiving 1 bit are operated on the rising edge of the clock.

4.4.1、Write Data



4.4.2、Read Data

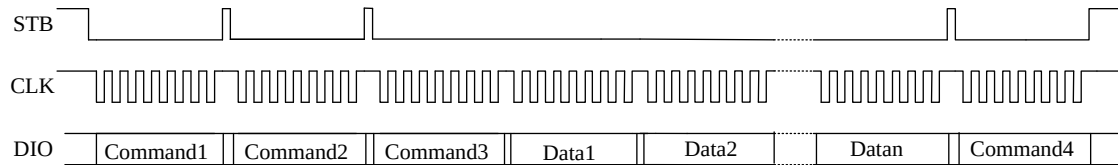


Note: When reading data, starting from the eighth rising edges of the serial clock CLK, there is a waiting time t_{WAIT} (minimum 1us) between the read data and the CLK falling edge.



4.5、The Transmission Of Serial Data In Application

4.5.1、Address Increase Mode Communication Timing



Command1: Display mode setting

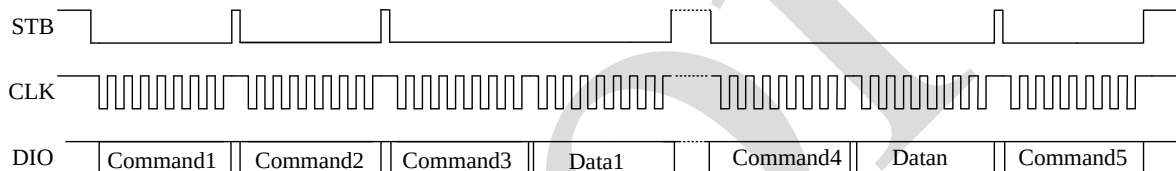
Command2: Data command setting

Command3: Address command setting

Data1~Datan: Display data

Command4: Display control command setting

4.5.2、Fixed Address Mode Communication Timing



Command1: Display mode setting

Command2: Data command setting

Command3: Address 1 command setting

Data1: Display data 1

⋮

Command4: Address N command setting

Datan: Display data n

Command5: Display control command setting

4.5.3、Reading Key Timing

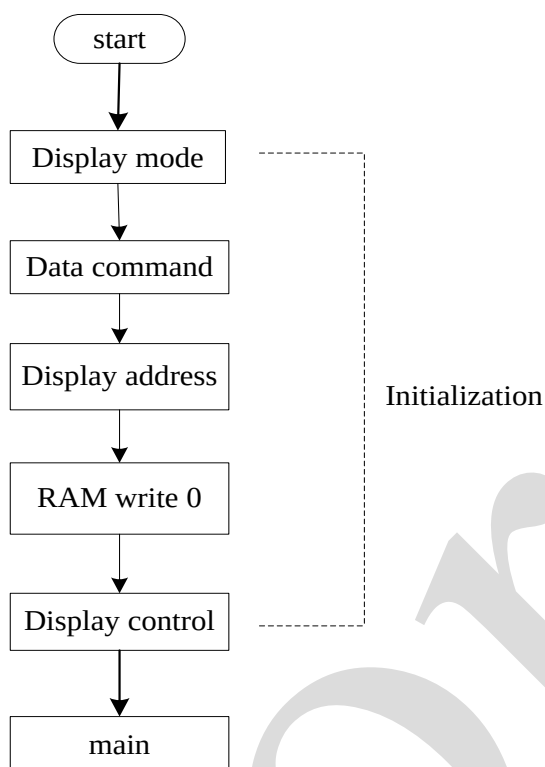


Command1: Setting the reading key command

Data1~4: Read key data



4.6、Initialization Flow Chart

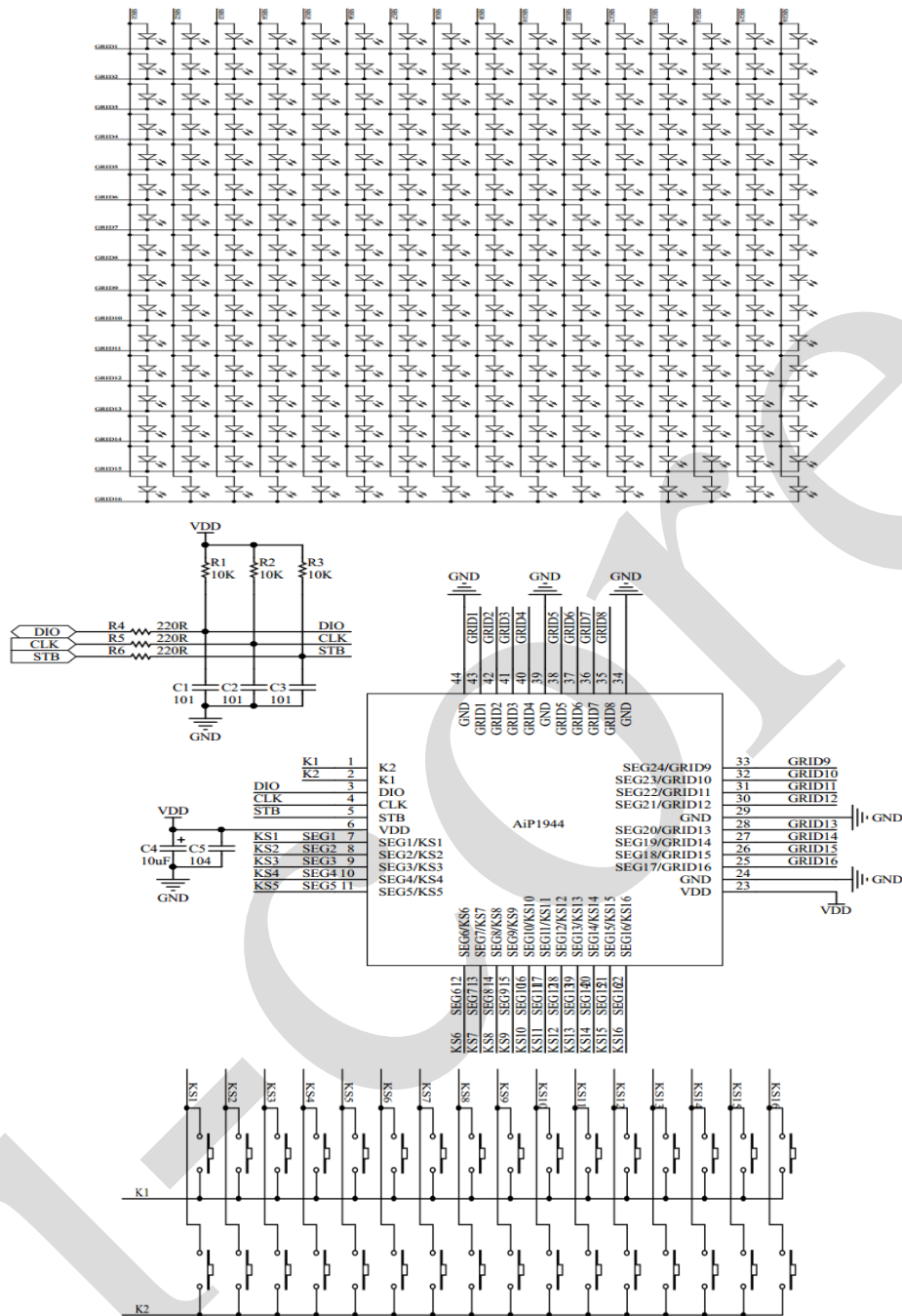


Note:

1. The display mode setting is used to select the segment number of the driver's display screen. It is selected according to the actual hardware connection of the user, and it is usually set in the initialization part.
2. the data instruction is used to select the RAM area to write the display data (two types are added to the fixed address and address) or read key keys.
3. IC in power on the display RAM content is not fixed, in order to prevent the user first display when the display appears disorderly. It is suggested that the RAM should be emptied before opening the display.



5、Typical Application Circuit



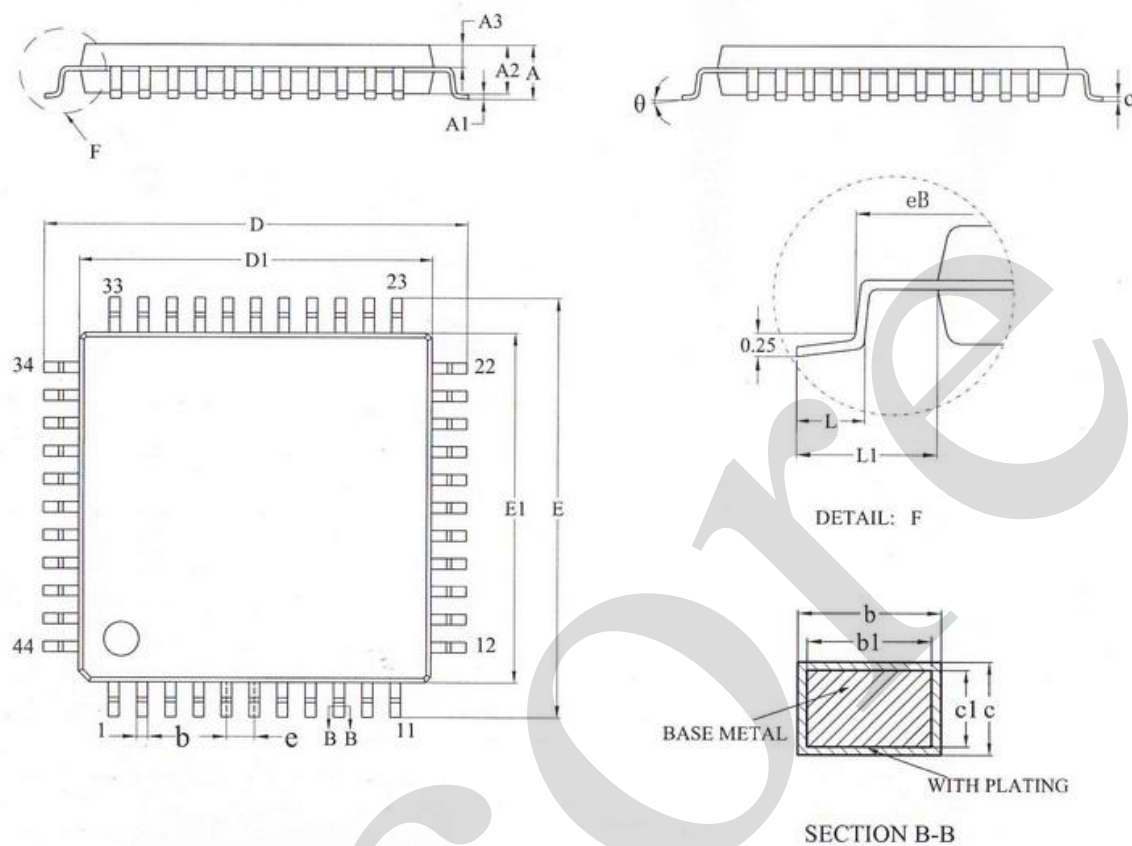
Application Note:

- 1, the filter capacitance between VDD and GND should be close to AiP1944 to enhance the filtering effect.
2. In order to improve the anti-interference ability of the circuit, the communication port is suggested to be connected according to the above diagram, and the specific parameters can be adjusted according to the actual needs.



6、Package Information

6.1、LQFP44



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.80BSC		
eB	11.25	—	11.45
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°



7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notion

Recommended carefully reading this information before the use of this product;

The information in this document are subject to change without notice;

This information is using to the reference only, the company is not responsible for any loss;

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