



AiP74AVC4T774

4-bit Dual Supply Translating Transceiver; 3-state

Product Specification

Specification Revision History:

Version	Date	Description
2019-10-A1	2019-10	New
2023-04-B1	2023-04	Update the template
2026-03-B2	2026-03	Add MIS16 package form; add ESD; update package information



Contents

1、General Description.....	1
2、Block Diagram And Pin Description	3
2.1、Block Diagram	3
2.2、Pin Configurations.....	3
2.3、Pin Description.....	4
2.4、Function Table.....	4
3、Electrical Parameter	5
3.1、Absolute Maximum Ratings.....	5
3.2、Recommended Operating Conditions.....	5
3.3、Electrical Characteristics.....	6
3.3.1、DC Characteristics 1.....	6
3.3.2、DC Characteristics 2.....	7
3.3.3、DC Characteristics 3.....	9
3.3.4、AC Characteristics 1.....	11
3.3.5、AC Characteristics 2.....	12
3.3.6、AC Characteristics 3.....	12
3.3.7、AC Characteristics 4.....	13
3.3.8、AC Characteristics 5.....	14
4.1、AC Testing Circuit	15
4.2、AC Testing Waveforms.....	15
4.3、Measurement Points	16
4.4、Test Data	16
5、Characteristic Curve.....	17
6、Package Information	21
6.1、TSSOP16.....	21
6.2、DHVQFN16	22
6.3、MIS16.....	23
7、Statements And Notes	24
7.1、The name and content of Hazardous substances or Elements in the product	24
7.2、Notes	24



1、General Description

The AiP74AVC4T774 is a 4-bit, dual supply transceiver that enables bidirectional level translation. It features eight 1-bit input-output ports (A_n and B_n), four direction control inputs (DIR1, DIR2, DIR3 and DIR4), an output enable input ($\overline{OE}$) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 0.8V and 3.6V making the device suitable for translating between any of the low voltage nodes (0.8V, 1.2V, 1.5V, 1.8V, 2.5V and 3.3V). Pins A_n , $\overline{OE}$ and DIRn are referenced to $V_{CC(A)}$ and pins B_n are referenced to $V_{CC(B)}$. A HIGH on DIRn allows transmission from A_n to B_n and a LOW on DIRn allows transmission from B_n to A_n . The output enable input ($\overline{OE}$) can be used to disable the outputs so the buses are effectively isolated.

The device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A_n and B_n are in the high-impedance OFF-state.

Features:

- Wide supply voltage range:
 $V_{CC(A)}$: 0.8V to 3.6V
 $V_{CC(B)}$: 0.8V to 3.6V
- Suspend mode
- Inputs accept voltages up to 3.6V
- I_{OFF} circuitry provides partial Power-down mode operation
- Specified from -40°C to +125°C
- Packaging information: TSSOP16/DHVQFN16/MIS16

**Ordering Information:****Tube packing specifications:**

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74AVC4T774TA16.TB	TSSOP16	74AVC4T774	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74AVC4T774TA16.TR	TSSOP16	74AVC4T774	5000PCS/reel	10000PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74AVC4T774QE16.TR	DHVQFN16	AVC4T774	3000PCS/reel	3000PCS/box	Dimensions of plastic enclosure: 2.5mm×3.5mm Pin spacing: 0.5mm
AiP74AVC4T774MIS16.TR	MIS16	AVC4T774	3000PCS/reel	30000PCS/box	Dimensions of plastic enclosure: 2.6mm×1.8mm Pin spacing: 0.4mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



2、Block Diagram And Pin Description

2.1、Block Diagram

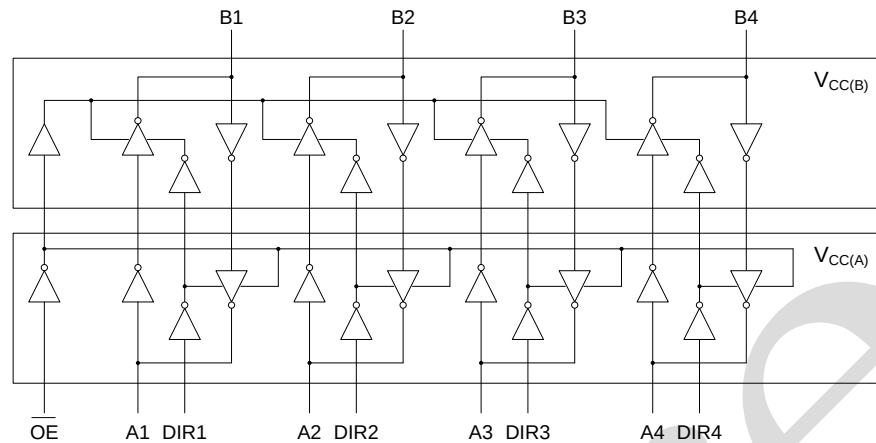


Figure 1. Logic symbol

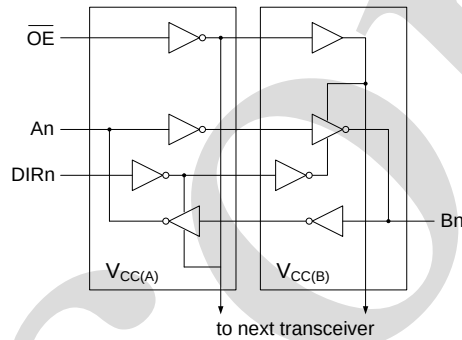
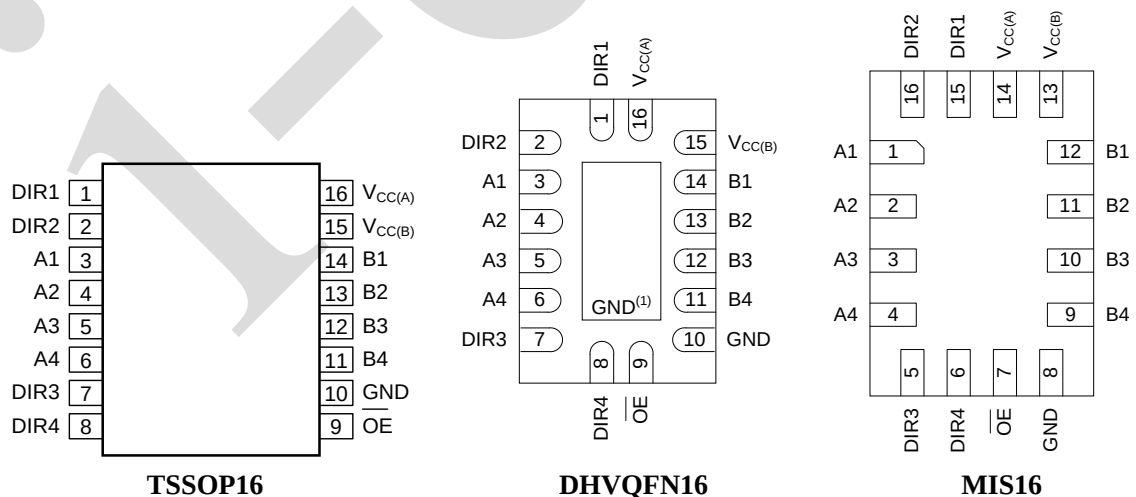


Figure 2. Logic diagram (one 1-bit transceiver)

2.2、Pin Configurations



Note: (1) This is not a supply pin, the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However if it is soldered the solder land should remain floating or be connected to GND.



2.3、Pin Description

Pin No.		Pin Name	Description
TSSOP16/DHVQFN16	MIS16		
1	15	DIR1	direction control input
2	16	DIR2	direction control input
3	1	A1	data input or output
4	2	A2	data input or output
5	3	A3	data input or output
6	4	A4	data input or output
7	5	DIR3	direction control input
8	6	DIR4	direction control input
9	7	$\overline{\text{OE}}$	output enable input (active LOW)
10	8	GND	ground (0V)
11	9	B4	data input or output
12	10	B3	data input or output
13	11	B2	data input or output
14	12	B1	data input or output
15	13	$V_{CC(B)}$	supply voltage B (Bn inputs are referenced to $V_{CC(B)}$)
16	14	$V_{CC(A)}$	supply voltage A (An, $\overline{\text{OE}}$ and DIRn inputs are referenced to $V_{CC(A)}$)

2.4、Function Table

Supply voltage	Input					Input/Output	
$V_{CC(A)}, V_{CC(B)}$	$\overline{\text{OE}}$	DIR1	DIR2	DIR3	DIR4	An	Bn
0.8V to 3.6V	L	L	X	X	X	A1=B1	input B1
0.8V to 3.6V	L	H	X	X	X	input A1	B1=A1
0.8V to 3.6V	L	X	L	X	X	A2=B2	input B2
0.8V to 3.6V	L	X	H	X	X	input A2	B2=A2
0.8V to 3.6V	L	X	X	L	X	A3=B3	input B3
0.8V to 3.6V	L	X	X	H	X	input A3	B3=A3
0.8V to 3.6V	L	X	X	X	L	A4=B4	input B4
0.8V to 3.6V	L	X	X	X	H	input A4	B4=A4
0.8V to 3.6V	H	X	X	X	X	Z	Z
GND	X	X	X	X	X	Z	Z

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

[2] The An, DIRn and $\overline{\text{OE}}$ input circuit is referenced to $V_{CC(A)}$; The Bn input circuit is referenced to $V_{CC(B)}$.

[3] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.



3、Electrical Parameter

3.1、Absolute Maximum Ratings

($T_{amb}=25^{\circ}\text{C}$, all voltage referenced to GND, unless otherwise specified)

Characteristic	Symbol	Conditions	Min.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	-0.5	+4.6	V
supply voltage B	$V_{CC(B)}$	-	-0.5	+4.6	V
input clamping current	I_{IK}	$V_I < 0\text{V}$	-50	-	mA
input voltage	V_I	[1]	-0.5	+4.6	V
output clamping current	I_{IK}	$V_O < 0\text{V}$	-50	-	mA
output voltage	V_O	Active mode ^{[1][2][3]}	-0.5	$V_{CCO}+0.5$	V
		Suspend or 3-state mode ^[1]	-0.5	+4.6	V
output current	I_O	$V_O=0\text{V}$ to V_{CCO} ^[2]	-	± 50	mA
supply current	I_{CC}	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
ground current	I_{GND}	-	-100	-	mA
storage temperature	T_{stg}	-	-65	+150	$^{\circ}\text{C}$
total power dissipation	P_{tot}	-	-	500	mW
soldering temperature	T_L	10s	260		$^{\circ}\text{C}$
electrostatic discharge	ESD	HBM	2000		V

Note:

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] $V_{CCO}+0.5\text{V}$ should not exceed 4.6V.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	0.8	-	3.6	V
supply voltage B	$V_{CC(B)}$	-	0.8	-	3.6	V
input voltage	V_I	-	0	-	3.6	V
output voltage	V_O	Active mode ^[1]	0	-	V_{CCO}	V
		Suspend or 3-state mode	0	-	3.6	V
ambient temperature	T_{amb}	-	-40	-	+125	$^{\circ}\text{C}$
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CCI}=0.8\text{V}$ to 3.6V ^[2]	-	-	10	ns/V

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the input port.



3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified)^{[1][2]}

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HIGH-level output voltage	V_{OH}	$V_I=V_{IH}$ or V_{IL} $I_O=-1.5\text{mA}$; $V_{CC(A)}=V_{CC(B)}=0.8\text{V}$	-	0.69	-	V
LOW-level output voltage	V_{OL}	$V_I=V_{IH}$ or V_{IL} $I_O=1.5\text{mA}$; $V_{CC(A)}=V_{CC(B)}=0.8\text{V}$	-	0.07	-	V
input leakage current	I_I	DIRn, $\overline{OE}$ input; $V_I=0\text{V}$ or 3.6V ; $V_{CC(A)}=V_{CC(B)}=0.8\text{V}$ to 3.6V	-	-	± 1	μA
OFF-state output current	I_{OZ}	A or B port; $V_O=0\text{V}$ or V_{CCO} ; $V_{CC(A)}=V_{CC(B)}=3.6\text{V}$ ^[3]	-	-	± 2.5	μA
		suspend mode A port; $V_O=0\text{V}$ or V_{CCO} ; $V_{CC(A)}=3.6\text{V}$; $V_{CC(B)}=0\text{V}$ ^[3]	-	-	± 2.5	μA
		suspend mode B port; $V_O=0\text{V}$ or V_{CCO} ; $V_{CC(A)}=0\text{V}$; $V_{CC(B)}=3.6\text{V}$ ^[3]	-	-	± 2.5	μA
power-off leakage current	I_{OFF}	A port; V_I or $V_O=0\text{V}$ to 3.6V ; $V_{CC(A)}=0\text{V}$; $V_{CC(B)}=0.8\text{V}$ to 3.6V	-	-	± 1	μA
		B port; V_I or $V_O=0\text{V}$ to 3.6V ; $V_{CC(B)}=0\text{V}$; $V_{CC(A)}=0.8\text{V}$ to 3.6V	-	-	± 1	μA
input capacitance	C_I	DIRn, $\overline{OE}$ input; $V_I=0\text{V}$ or 3.3V ; $V_{CC(A)}=V_{CC(B)}=3.3\text{V}$	-	2.0	-	pF
input/output capacitance	$C_{I/O}$	A and B port; $V_O=3.3\text{V}$ or 0V ; $V_{CC(A)}=V_{CC(B)}=3.3\text{V}$	-	4.0	-	pF

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.



3.3.2、DC Characteristics 2

($T_{amb}=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified) ^{[1][2]}

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	data input	$V_{CCI}=0.8\text{V}$	$0.70V_{CCI}$	-	V
			$V_{CCI}=1.1\text{V to }1.95\text{V}$	$0.65V_{CCI}$	-	V
			$V_{CCI}=2.3\text{V to }2.7\text{V}$	1.6	-	V
			$V_{CCI}=3.0\text{V to }3.6\text{V}$	2	-	V
		DIRn, OE input	$V_{CC(A)}=0.8\text{V}$	$0.70V_{CC(A)}$	-	V
			$V_{CC(A)}=1.1\text{V to }1.95\text{V}$	$0.65V_{CC(A)}$	-	V
			$V_{CC(A)}=2.3\text{V to }2.7\text{V}$	1.6	-	V
			$V_{CC(A)}=3.0\text{V to }3.6\text{V}$	2	-	V
LOW-level input voltage	V_{IL}	data input	$V_{CCI}=0.8\text{V}$	-	$0.30V_{CCI}$	V
			$V_{CCI}=1.1\text{V to }1.95\text{V}$	-	$0.35V_{CCI}$	V
			$V_{CCI}=2.3\text{V to }2.7\text{V}$	-	0.7	V
			$V_{CCI}=3.0\text{V to }3.6\text{V}$	-	0.8	V
		DIRn, OE input	$V_{CC(A)}=0.8\text{V}$	-	$0.30V_{CC(A)}$	V
			$V_{CC(A)}=1.1\text{V to }1.95\text{V}$	-	$0.35V_{CC(A)}$	V
			$V_{CC(A)}=2.3\text{V to }2.7\text{V}$	-	0.7	V
			$V_{CC(A)}=3.0\text{V to }3.6\text{V}$	-	0.8	V
HIGH-level output voltage	V_{OH}	$V_I=V_{IH} \text{ or } V_{IL}$	$I_O=-100\mu\text{A};$ $V_{CC(A)}=V_{CC(B)}=0.8\text{V to }3.6\text{V}$	$V_{CCO}-0.1$	-	V
			$I_O=-3\text{mA};$ $V_{CC(A)}=V_{CC(B)}=1.1\text{V}$	0.85	-	V
			$I_O=-6\text{mA};$ $V_{CC(A)}=V_{CC(B)}=1.4\text{V}$	1.05	-	V
			$I_O=-8\text{mA};$ $V_{CC(A)}=V_{CC(B)}=1.65\text{V}$	1.2	-	V
			$I_O=-9\text{mA};$ $V_{CC(A)}=V_{CC(B)}=2.3\text{V}$	1.75	-	V
			$I_O=-12\text{mA};$ $V_{CC(A)}=V_{CC(B)}=3.0\text{V}$	2.3	-	V
LOW-level output voltage	V_{OL}	$V_I=V_{IH} \text{ or } V_{IL}$	$I_O=100\mu\text{A};$ $V_{CC(A)}=V_{CC(B)}=0.8\text{V to }3.6\text{V}$	-	0.1	V
			$I_O=3\text{mA};$ $V_{CC(A)}=V_{CC(B)}=1.1\text{V}$	-	0.25	V
			$I_O=6\text{mA};$ $V_{CC(A)}=V_{CC(B)}=1.4\text{V}$	-	0.35	V
			$I_O=8\text{mA};$ $V_{CC(A)}=V_{CC(B)}=1.65\text{V}$	-	0.45	V
			$I_O=9\text{mA};$ $V_{CC(A)}=V_{CC(B)}=2.3\text{V}$	-	0.55	V
			$I_O=12\text{mA};$ $V_{CC(A)}=V_{CC(B)}=3.0\text{V}$	-	0.7	V
input leakage current	I_I	DIRn, OE input; $V_I=0\text{V}$ or $3.6\text{V};$ $V_{CC(A)}=V_{CC(B)}=0.8\text{V to }3.6\text{V}$	-	-	± 1	μA



OFF-state output current	I_{OZ}	A or B port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=V_{CC(B)}=3.6V^{[3]}$		-	-	± 5	μA
		suspend mode A port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=3.6V$; $V_{CC(B)}=0V^{[3]}$		-	-	± 5	μA
		suspend mode B port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=0V$; $V_{CC(B)}=3.6V^{[3]}$		-	-	± 5	μA
power-off leakage current	I_{OFF}	A port; V_I or $V_O=0V$ to $3.6V$; $V_{CC(A)}=0V$; $V_{CC(B)}=0.8V$ to $3.6V$		-	-	± 5	μA
		B port; V_I or $V_O=0V$ to $3.6V$; $V_{CC(B)}=0V$; $V_{CC(A)}=0.8V$ to $3.6V$		-	-	± 5	μA
supply current	I_{CC}	A port; $V_I=0V$ or V_{CCI} ; $I_O=0A$	$V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$	-	-	10	μA
			$V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$	-	-	8	μA
			$V_{CC(A)}=3.6V$; $V_{CC(B)}=0V$	-	-	8	μA
			$V_{CC(A)}=0V$; $V_{CC(B)}=3.6V$	-2	-	-	μA
		B port; $V_I=0V$ or V_{CCI} ; $I_O=0A$	$V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$	-	-	10	μA
			$V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$	-	-	8	μA
			$V_{CC(A)}=3.6V$; $V_{CC(B)}=0V$	-2	-	-	μA
			$V_{CC(A)}=0V$; $V_{CC(B)}=3.6V$	-	-	8	μA
		A plus B port ($I_{CC(A)}+I_{CC(B)}$); $I_O=0A$; $V_I=0V$ or V_{CCI} ; $V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$		-	-	20	μA
		A plus B port ($I_{CC(A)}+I_{CC(B)}$); $I_O=0A$; $V_I=0V$ or V_{CCI} ; $V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$		-	-	16	μA
Additional supply current	ΔI_{CC}	$V_I=3.0V$; $V_{CC(A)}=V_{CC(B)}=3.6V$		-	-	500	μA

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.



3.3.3、DC Characteristics 3

($T_{amb}=-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified) ^{[1][2]}

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	data input	$V_{CCI}=0.8\text{V}$	$0.70V_{CCI}$	-	V
			$V_{CCI}=1.1\text{V to }1.95\text{V}$	$0.65V_{CCI}$	-	V
			$V_{CCI}=2.3\text{V to }2.7\text{V}$	1.6	-	V
			$V_{CCI}=3.0\text{V to }3.6\text{V}$	2	-	V
		DIRn, OE input	$V_{CC(A)}=0.8\text{V}$	$0.70V_{CC(A)}$	-	V
			$V_{CC(A)}=1.1\text{V to }1.95\text{V}$	$0.65V_{CC(A)}$	-	V
			$V_{CC(A)}=2.3\text{V to }2.7\text{V}$	1.6	-	V
			$V_{CC(A)}=3.0\text{V to }3.6\text{V}$	2	-	V
LOW-level input voltage	V_{IL}	data input	$V_{CCI}=0.8\text{V}$	-	$0.30V_{CCI}$	V
			$V_{CCI}=1.1\text{V to }1.95\text{V}$	-	$0.35V_{CCI}$	V
			$V_{CCI}=2.3\text{V to }2.7\text{V}$	-	0.7	V
			$V_{CCI}=3.0\text{V to }3.6\text{V}$	-	0.8	V
		DIRn, OE input	$V_{CC(A)}=0.8\text{V}$	-	$0.30V_{CC(A)}$	V
			$V_{CC(A)}=1.1\text{V to }1.95\text{V}$	-	$0.35V_{CC(A)}$	V
			$V_{CC(A)}=2.3\text{V to }2.7\text{V}$	-	0.7	V
			$V_{CC(A)}=3.0\text{V to }3.6\text{V}$	-	0.8	V
HIGH-level output voltage	V_{OH}	$V_I=V_{IH}$ or V_{IL}	$I_O=-100\mu\text{A}; V_{CC(A)}=V_{CC(B)}=0.8\text{V to }3.6\text{V}$	$V_{CCO}-0.1$	-	V
			$I_O=-3\text{mA}; V_{CC(A)}=V_{CC(B)}=1.1\text{V}$	0.85	-	V
			$I_O=-6\text{mA}; V_{CC(A)}=V_{CC(B)}=1.4\text{V}$	1.05	-	V
			$I_O=-8\text{mA}; V_{CC(A)}=V_{CC(B)}=1.65\text{V}$	1.2	-	V
			$I_O=-9\text{mA}; V_{CC(A)}=V_{CC(B)}=2.3\text{V}$	1.75	-	V
			$I_O=-12\text{mA}; V_{CC(A)}=V_{CC(B)}=3.0\text{V}$	2.3	-	V
LOW-level output voltage	V_{OL}	$V_I=V_{IH}$ or V_{IL}	$I_O=100\mu\text{A}; V_{CC(A)}=V_{CC(B)}=0.8\text{V to }3.6\text{V}$	-	0.1	V
			$I_O=3\text{mA}; V_{CC(A)}=V_{CC(B)}=1.1\text{V}$	-	0.25	V
			$I_O=6\text{mA}; V_{CC(A)}=V_{CC(B)}=1.4\text{V}$	-	0.35	V
			$I_O=8\text{mA}; V_{CC(A)}=V_{CC(B)}=1.65\text{V}$	-	0.45	V
			$I_O=9\text{mA}; V_{CC(A)}=V_{CC(B)}=2.3\text{V}$	-	0.55	V
			$I_O=12\text{mA}; V_{CC(A)}=V_{CC(B)}=3.0\text{V}$	-	0.7	V
input leakage current	I_I	DIRn, OE input; $V_I=0\text{V}$ or $3.6\text{V}; V_{CC(A)}=V_{CC(B)}=0.8\text{V to }3.6\text{V}$	-	-	± 5	μA



OFF-state output current	I_{OZ}	A or B port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=V_{CC(B)}=3.6V^{[3]}$		-	-	± 30	μA
		suspend mode A port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=3.6V$; $V_{CC(B)}=0V^{[3]}$		-	-	± 30	μA
		suspend mode B port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=0V$; $V_{CC(B)}=3.6V^{[3]}$		-	-	± 30	μA
power-off leakage current	I_{OFF}	A port; V_I or $V_O=0V$ to $3.6V$; $V_{CC(A)}=0V$; $V_{CC(B)}=0.8V$ to $3.6V$		-	-	± 30	μA
		B port; V_I or $V_O=0V$ to $3.6V$; $V_{CC(B)}=0V$; $V_{CC(A)}=0.8V$ to $3.6V$		-	-	± 30	μA
supply current	I_{CC}	A port; $V_I=0V$ or V_{CCI} ; $I_O=0A$	$V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$	-	-	55	μA
			$V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$	-	-	50	μA
			$V_{CC(A)}=3.6V$; $V_{CC(B)}=0V$	-	-	50	μA
			$V_{CC(A)}=0V$; $V_{CC(B)}=3.6V$	-12	-	-	μA
		B port; $V_I=0V$ or V_{CCI} ; $I_O=0A$	$V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$	-	-	55	μA
			$V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$	-	-	50	μA
			$V_{CC(A)}=3.6V$; $V_{CC(B)}=0V$	-12	-	-	μA
			$V_{CC(A)}=0V$; $V_{CC(B)}=3.6V$	-	-	50	μA
		A plus B port ($I_{CC(A)}+I_{CC(B)}$); $I_O=0A$; $V_I=0V$ or V_{CCI} ; $V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$		-	-	70	μA
		A plus B port ($I_{CC(A)}+I_{CC(B)}$); $I_O=0A$; $V_I=0V$ or V_{CCI} ; $V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$		-	-	65	μA
Additional supply current	ΔI_{CC}	$V_I=3.0V$; $V_{CC(A)}=V_{CC(B)}=3.6V$		-	-	650	μA

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.

**Typical total supply current ($I_{CC(A)}+I_{CC(B)}$)**

$V_{CC(A)}$	$V_{CC(B)}$							Unit
	0V	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
0V	0	0.1	0.1	0.1	0.1	0.1	0.1	uA
0.8V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	uA
1.2V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	uA
1.5V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	uA
1.8V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	uA
2.5V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	uA
3.3V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	uA

3.3.4、AC Characteristics 1(T_{amb}=25℃, V_{CC(A)}=V_{CC(B)}, voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions	$V_{CC(A)}=V_{CC(B)}$						Unit
			0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
power dissipation capacitance	C _{PD}	A port: (direction An to Bn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction An to Bn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction Bn to An); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		A port: (direction Bn to An); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction An to Bn); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		B port: (direction An to Bn); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction Bn to An); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction Bn to An); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

Note:

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in uW). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:f_i=input frequency in MHz;f_o=output frequency in MHz;C_L=load capacitance in pF;V_{CC}=supply voltage in V;

N=number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ =sum of the outputs.[2] f_i=10MHz; V_I=GND to V_{CC}; t_r=t_f=1ns; C_L=0pF; R_L=∞Ω.



3.3.5、AC Characteristics 2

($T_{amb}=25^{\circ}\text{C}$, $V_{CC(A)}=0.8\text{V}$, voltages are referenced to GND (ground=0V), unless otherwise specified)^[1]

Parameter	Symbol	Conditions	$V_{CC(B)}$						Unit
			0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
propagation delay	t_{pd}	An to Bn	14.5	7.3	6.5	6.2	5.9	6.0	ns
		Bn to An	14.5	12.7	12.4	12.3	12.1	12.0	ns
disable time	t_{dis}	$\overline{\text{OE}}$ to An	14.3	14.3	14.3	14.3	14.3	14.3	ns
		$\overline{\text{OE}}$ to Bn	17.0	9.9	9.0	9.4	9.0	9.7	ns
enable time	t_{en}	$\overline{\text{OE}}$ to An	18.2	18.2	18.2	18.2	18.2	18.2	ns
		$\overline{\text{OE}}$ to Bn	19.2	10.7	9.8	9.6	9.7	10.2	ns

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

3.3.6、AC Characteristics 3

($T_{amb}=25^{\circ}\text{C}$, $V_{CC(B)}=0.8\text{V}$, voltages are referenced to GND (ground=0V), unless otherwise specified)^[1]

Parameter	Symbol	Conditions	$V_{CC(A)}$						Unit
			0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
propagation delay	t_{pd}	An to Bn	14.5	12.7	12.4	12.3	12.1	12.0	ns
		Bn to An	14.5	7.3	6.5	6.2	5.9	6.0	ns
disable time	t_{dis}	$\overline{\text{OE}}$ to An	14.3	5.5	4.1	4.0	3.0	3.5	ns
		$\overline{\text{OE}}$ to Bn	17.0	13.8	13.4	13.1	12.9	12.7	ns
enable time	t_{en}	$\overline{\text{OE}}$ to An	18.2	5.6	4.0	3.2	2.4	2.2	ns
		$\overline{\text{OE}}$ to Bn	19.2	14.6	14.1	13.9	13.7	13.6	ns

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .



3.3.7、AC Characteristics 4

($T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified)^[1]

Parameter	Symbol	Conditions	V _{CC(B)}										Unit
			1.2V ±0.1V		1.5V ±0.1V		1.8V ±0.15V		2.5V ±0.2V		3.3V ±0.3V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V _{CC(A)} =1.1V to 1.3V													
propagation delay	t _{pd}	An to Bn	2.0	10.5	1.3	7.8	1.2	6.9	1.0	5.9	0.8	5.7	ns
		Bn to An	2.0	10.5	1.5	9.9	1.5	9.7	1.4	9.4	1.4	9.3	ns
disable time	t _{dis}	$\overline{OE}$ to An	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	ns
		$\overline{OE}$ to Bn	2.0	11.1	2.0	8.6	1.0	8.0	0.7	7.0	1.0	8.0	ns
enable time	t _{en}	$\overline{OE}$ to An	2.0	13.5	2.0	13.5	2.0	13.5	2.0	13.5	2.0	13.5	ns
		$\overline{OE}$ to Bn	2.0	15.0	2.0	11.0	2.0	9.4	1.0	7.8	1.0	7.4	ns
V _{CC(A)} =1.4V to 1.6V													
propagation delay	t _{pd}	An to Bn	1.5	9.9	1.0	7.1	1.0	6.0	0.5	4.8	0.5	4.3	ns
		Bn to An	1.3	7.8	1.0	7.1	0.9	6.9	0.8	6.6	0.6	6.5	ns
disable time	t _{dis}	$\overline{OE}$ to An	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	ns
		$\overline{OE}$ to Bn	2.0	10.2	1.5	7.5	0.9	7.2	0.4	6.2	0.4	6.1	ns
enable time	t _{en}	$\overline{OE}$ to An	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	ns
		$\overline{OE}$ to Bn	2.0	14.4	1.4	7.9	1.3	7.7	1.1	6.4	1.1	5.6	ns
V _{CC(A)} =1.65V to 1.95V													
propagation delay	t _{pd}	An to Bn	1.5	9.7	0.9	6.9	0.8	5.7	0.5	4.5	0.3	4.0	ns
		Bn to An	1.2	6.9	1.0	6.0	0.8	5.7	0.5	5.5	0.5	5.3	ns
disable time	t _{dis}	$\overline{OE}$ to An	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	ns
		$\overline{OE}$ to Bn	2.0	9.9	1.5	7.0	0.8	6.9	0.2	5.8	0.2	5.9	ns
enable time	t _{en}	$\overline{OE}$ to An	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	ns
		$\overline{OE}$ to Bn	1.5	13.9	1.2	7.2	1.2	6.9	0.8	5.4	0.6	5.0	ns
V _{CC(A)} =2.3V to 2.7V													
propagation delay	t _{pd}	An to Bn	1.4	9.4	0.8	6.6	0.5	5.5	0.4	4.2	0.2	3.7	ns
		Bn to An	1.0	5.9	0.5	4.8	0.5	4.5	0.4	4.2	0.3	3.9	ns
disable time	t _{dis}	$\overline{OE}$ to An	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	ns
		$\overline{OE}$ to Bn	2.0	9.3	1.5	6.7	0.7	6.3	0.2	5.0	0.2	5.7	ns
enable time	t _{en}	$\overline{OE}$ to An	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	ns
		$\overline{OE}$ to Bn	1.5	13.6	1.0	6.8	1.0	6.0	0.8	4.6	0.6	4.2	ns
V _{CC(A)} =3.0V to 3.6V													
propagation delay	t _{pd}	An to Bn	1.4	9.3	0.6	6.5	0.5	5.3	0.3	3.9	0.2	3.5	ns
		Bn to An	0.8	5.7	0.5	4.3	0.3	4.0	0.2	3.7	0.2	3.5	ns
disable time	t _{dis}	$\overline{OE}$ to An	0.2	4.5	0.2	4.5	0.2	4.5	0.2	4.5	0.2	4.5	ns
		$\overline{OE}$ to Bn	2.0	9.0	1.5	6.4	0.7	6.1	0.2	4.8	0.2	5.6	ns
enable time	t _{en}	$\overline{OE}$ to An	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	ns
		$\overline{OE}$ to Bn	1.5	13.4	1.0	6.7	1.0	5.9	0.7	4.4	0.5	4.0	ns

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{pZL} and t_{pZH} .



3.3.8、AC Characteristics 5

(T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified)^[1]

Parameter	Symbol	Conditions	V _{CC(B)}										Unit
			1.2V ±0.1V		1.5V ±0.1V		1.8V ±0.15V		2.5V ±0.2V		3.3V ±0.3V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V _{CC(A)} =1.1V to 1.3V													
propagation delay	t _{pd}	An to Bn	2.0	12.1	1.3	9.0	1.2	8.0	1.0	6.8	0.8	6.6	ns
		Bn to An	2.0	12.1	1.5	11.4	1.5	11.2	1.4	10.9	1.4	10.7	ns
disable time	t _{dis}	$\overline{\text{OE}}$ to An	2.0	11.5	2.0	11.5	2.0	11.5	2.0	11.5	2.0	11.5	ns
		$\overline{\text{OE}}$ to Bn	2.0	12.8	2.0	9.9	1.0	9.2	0.7	8.1	1.0	9.2	ns
enable time	t _{en}	$\overline{\text{OE}}$ to An	2.0	15.6	2.0	15.6	2.0	15.6	2.0	15.6	2.0	15.6	ns
		$\overline{\text{OE}}$ to Bn	2.0	17.3	2.0	12.7	2.0	10.9	1.0	9.0	1.0	8.6	ns
V _{CC(A)} =1.4V to 1.6V													
propagation delay	t _{pd}	An to Bn	1.5	11.4	1.0	8.2	1.0	6.9	0.5	5.6	0.5	5.0	ns
		Bn to An	1.3	9.0	1.0	8.2	0.9	8.0	0.8	7.6	0.6	7.5	ns
disable time	t _{dis}	$\overline{\text{OE}}$ to An	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	ns
		$\overline{\text{OE}}$ to Bn	2.0	11.8	1.5	8.7	0.9	8.3	0.4	7.2	0.4	7.1	ns
enable time	t _{en}	$\overline{\text{OE}}$ to An	1.0	8.7	1.0	8.7	1.0	8.7	1.0	8.7	1.0	8.7	ns
		$\overline{\text{OE}}$ to Bn	2.0	16.6	1.4	9.1	1.3	8.9	1.1	7.4	1.1	6.5	ns
V _{CC(A)} =1.65V to 1.95V													
propagation delay	t _{pd}	An to Bn	1.5	11.2	0.9	8.0	0.8	6.6	0.5	5.2	0.3	4.6	ns
		Bn to An	1.2	8.0	1.0	6.9	0.8	6.6	0.5	6.4	0.5	6.1	ns
disable time	t _{dis}	$\overline{\text{OE}}$ to An	0.5	6.6	0.5	6.6	0.5	6.6	0.5	6.6	0.5	6.6	ns
		$\overline{\text{OE}}$ to Bn	2.0	11.4	1.5	8.1	0.8	8.0	0.2	6.7	0.2	6.8	ns
enable time	t _{en}	$\overline{\text{OE}}$ to An	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	ns
		$\overline{\text{OE}}$ to Bn	1.5	16.0	1.2	8.3	1.2	8.0	0.8	6.3	0.6	5.8	ns
V _{CC(A)} =2.3V to 2.7V													
propagation delay	t _{pd}	An to Bn	1.4	10.9	0.8	7.6	0.5	6.4	0.4	4.9	0.2	4.3	ns
		Bn to An	1.0	6.8	0.5	5.6	0.5	5.2	0.4	4.9	0.3	4.5	ns
disable time	t _{dis}	$\overline{\text{OE}}$ to An	0.2	4.6	0.2	4.6	0.2	4.6	0.2	4.6	0.2	4.6	ns
		$\overline{\text{OE}}$ to Bn	2.0	10.7	1.5	7.8	0.7	7.3	0.2	5.8	0.2	6.6	ns
enable time	t _{en}	$\overline{\text{OE}}$ to An	0.6	5.2	0.6	5.2	0.6	5.2	0.6	5.2	0.6	5.2	ns
		$\overline{\text{OE}}$ to Bn	1.5	15.7	1.0	7.9	1.0	6.9	0.8	5.3	0.6	4.9	ns
V _{CC(A)} =3.0V to 3.6V													
propagation delay	t _{pd}	An to Bn	1.4	10.7	0.6	7.5	0.5	6.1	0.3	4.5	0.2	4.1	ns
		Bn to An	0.8	6.6	0.5	5.0	0.3	4.6	0.2	4.3	0.2	4.1	ns
disable time	t _{dis}	$\overline{\text{OE}}$ to An	0.2	5.2	0.2	5.2	0.2	5.2	0.2	5.2	0.2	5.2	ns
		$\overline{\text{OE}}$ to Bn	2.0	10.4	1.5	7.4	0.7	7.1	0.2	5.6	0.2	6.5	ns
enable time	t _{en}	$\overline{\text{OE}}$ to An	0.5	4.6	0.5	4.6	0.5	4.6	0.5	4.6	0.5	4.6	ns
		$\overline{\text{OE}}$ to Bn	1.5	15.5	1.0	7.8	1.0	6.8	0.7	5.1	0.5	4.6	ns

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{pZL} and t_{pZH}.



4、Testing Circuit

4.1、AC Testing Circuit

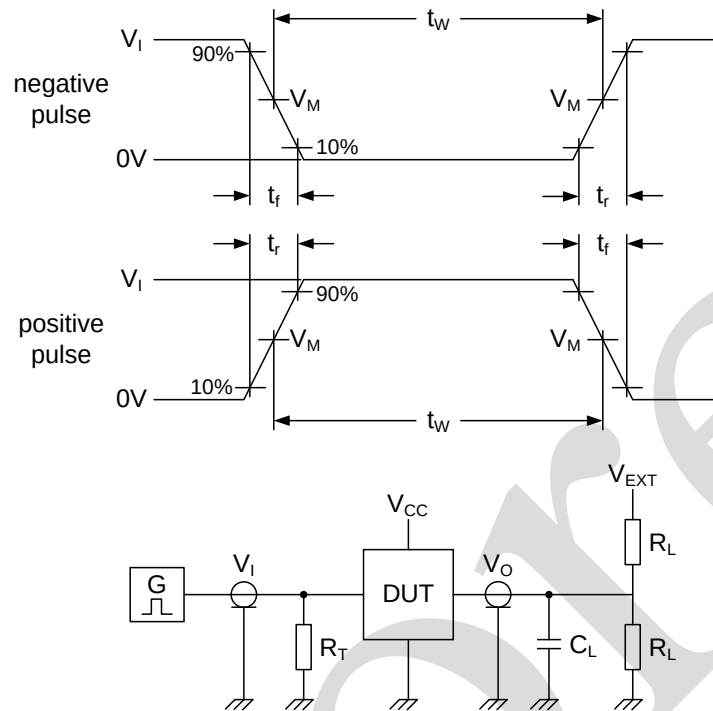


Figure 3. Test circuit for measuring switching times

R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} =External voltage for measuring switching times.

4.2、AC Testing Waveforms

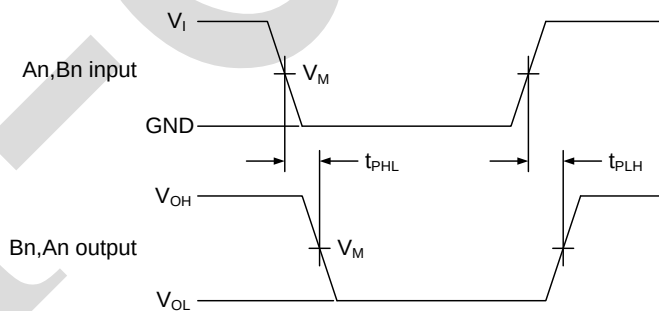


Figure 4. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times

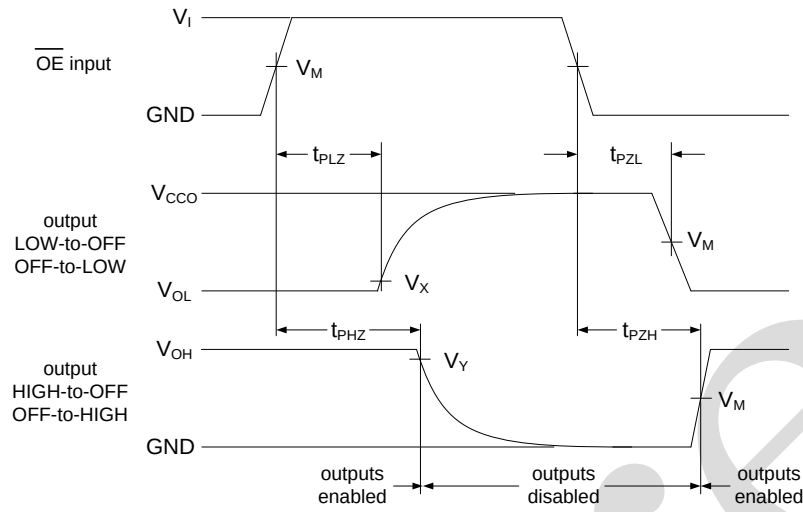


Figure 5. Enable and disable times

4.3、Measurement Points

Supply voltage	Input ^[1]	Output ^[2]		
$V_{CC(A)}, V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.8V to 1.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.1V$	$V_{OH}-0.1V$
1.65V to 2.7V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.15V$	$V_{OH}-0.15V$
3.0V to 3.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.3V$	$V_{OH}-0.3V$

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

4.4、Test Data

Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}, V_{CC(B)}$	$V_I^{[1]}$	$\Delta t/\Delta V^{[2]}$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	$t_{PZL}, t_{PLZ}^{[3]}$
0.8V to 1.6V	V_{CCI}	$\leq 1.0ns/V$	15pF	2k Ω	open	GND	$2V_{CCO}$
1.65V to 2.7V	V_{CCI}	$\leq 1.0ns/V$	15pF	2k Ω	open	GND	$2V_{CCO}$
3.0V to 3.6V	V_{CCI}	$\leq 1.0ns/V$	15pF	2k Ω	open	GND	$2V_{CCO}$

Note:

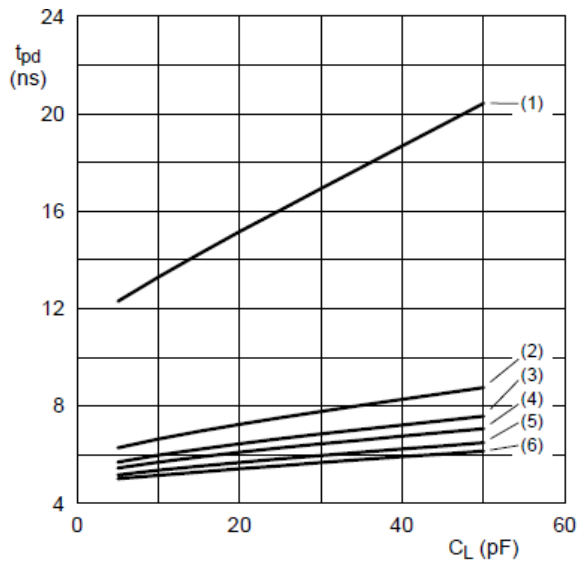
[1] V_{CCI} is the supply voltage associated with the data input port.

[2] $dV/dt \geq 1.0V/ns$

[3] V_{CCO} is the supply voltage associated with the output port.

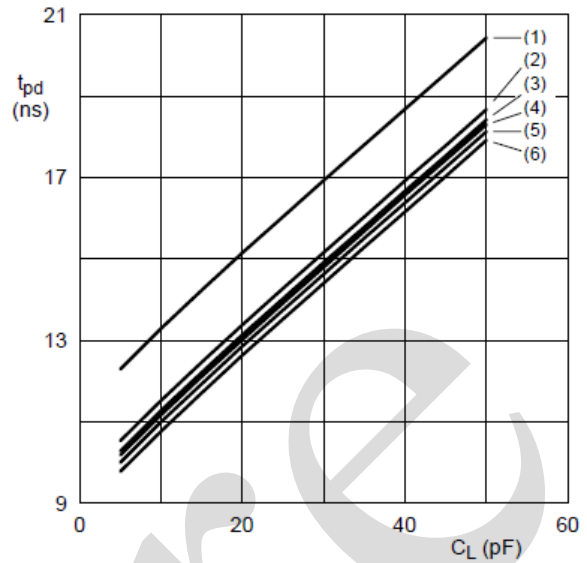


5、Characteristic Curve



a. Propagation delay (A to B); $V_{CC(A)}=0.8V$

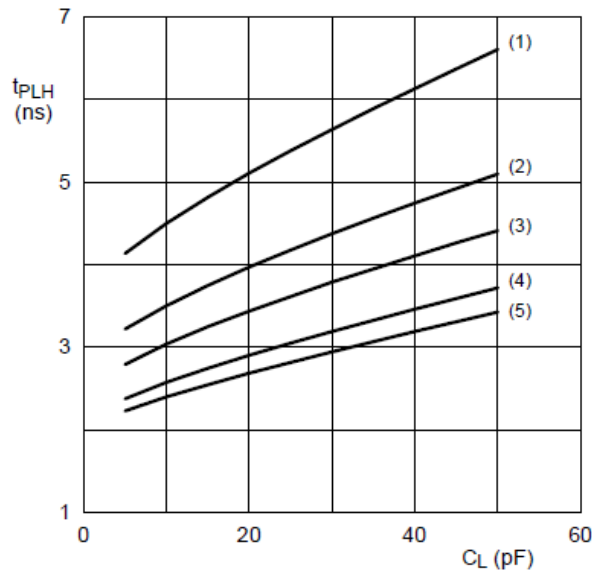
- (1) $V_{CC(B)}=0.8V$
- (2) $V_{CC(B)}=1.2V$
- (3) $V_{CC(B)}=1.5V$
- (4) $V_{CC(B)}=1.8V$
- (5) $V_{CC(B)}=2.5V$
- (6) $V_{CC(B)}=3.3V$



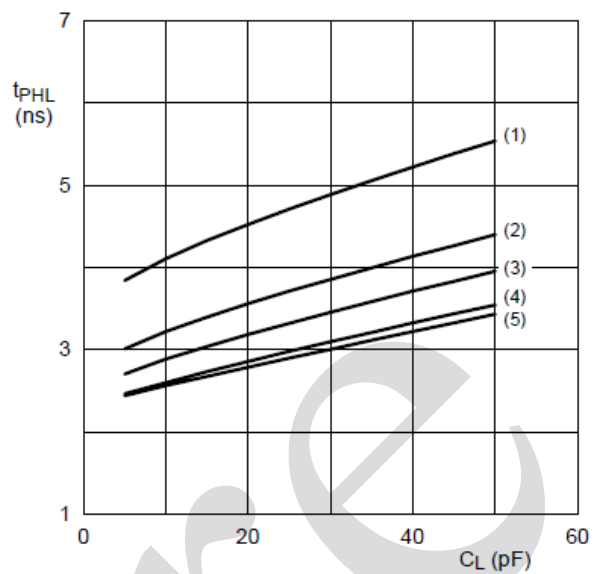
b. Propagation delay (A to B); $V_{CC(B)}=0.8V$

- (1) $V_{CC(B)}=0.8V$
- (2) $V_{CC(B)}=1.2V$
- (3) $V_{CC(B)}=1.5V$
- (4) $V_{CC(B)}=1.8V$
- (5) $V_{CC(B)}=2.5V$
- (6) $V_{CC(B)}=3.3V$

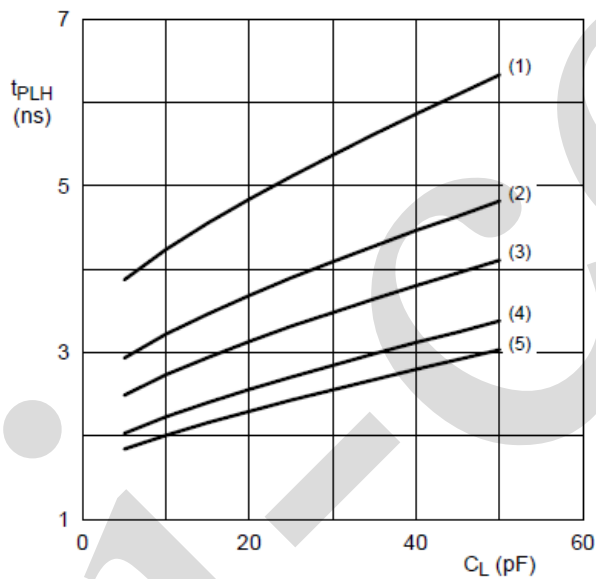
Figure 6. Typical propagation delay versus load capacitance; $T_{amb}=25^{\circ}C$



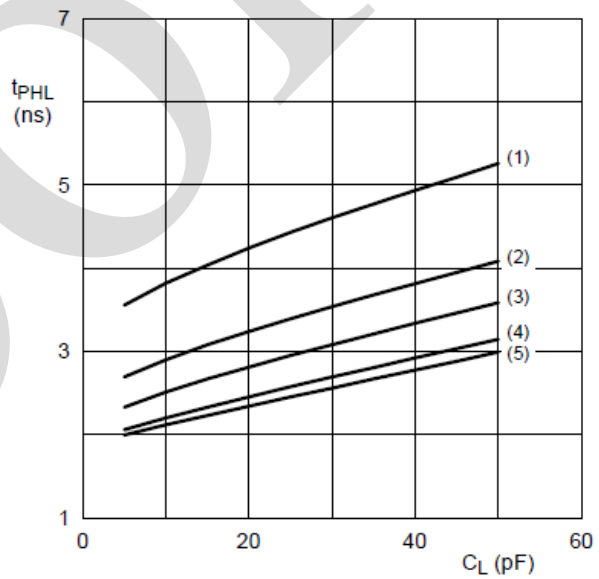
a. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=1.2V$



b. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=1.2V$

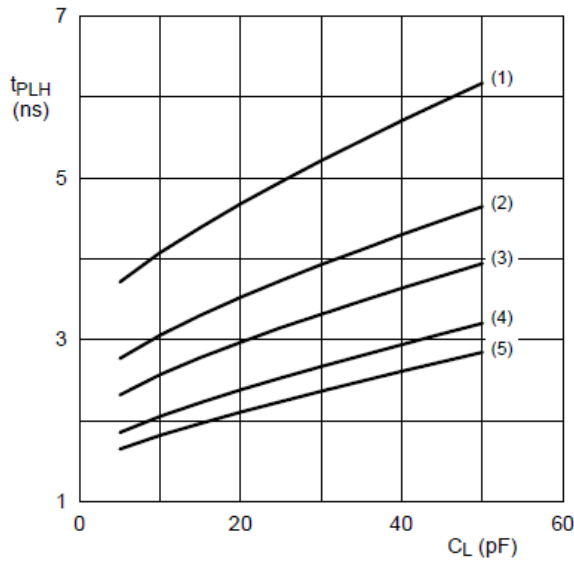


c. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=1.5V$
(1) $V_{CC(B)}=1.2V$
(2) $V_{CC(B)}=1.5V$
(3) $V_{CC(B)}=1.8V$
(4) $V_{CC(B)}=2.5V$
(5) $V_{CC(B)}=3.3V$

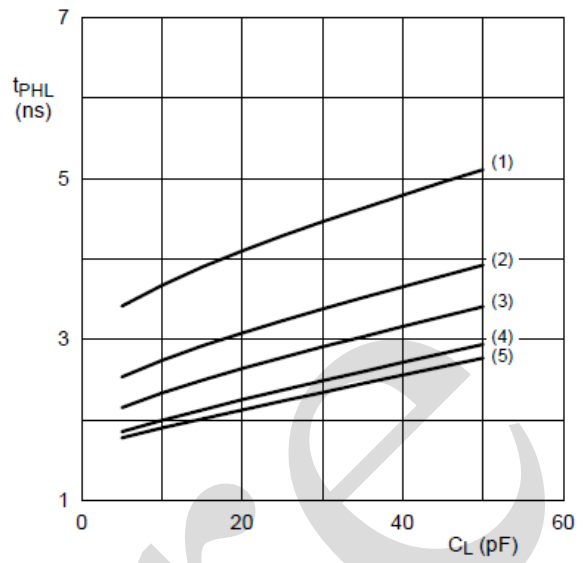


d. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=1.5V$

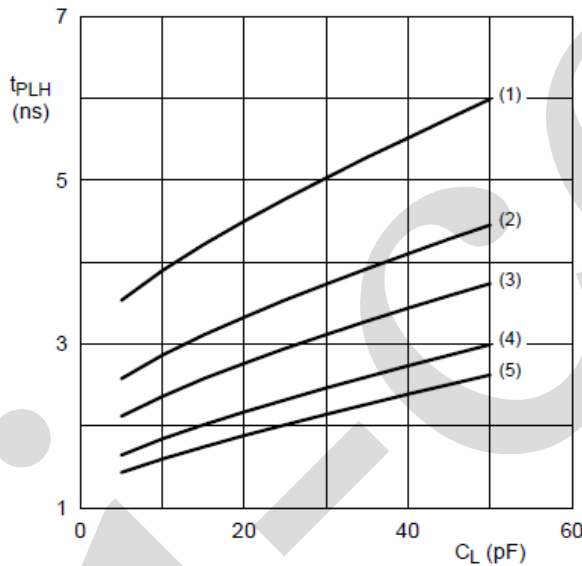
Figure 7. Typical propagation delay versus load capacitance; $T_{amb}=25^{\circ}C$



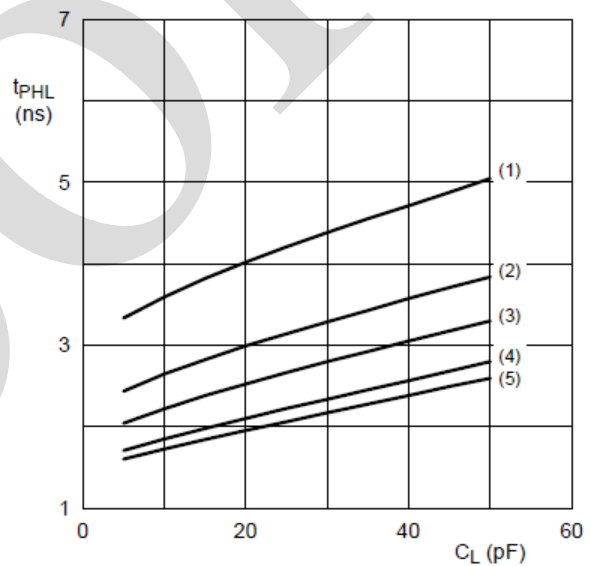
a. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 1.8V$



b. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 1.8V$

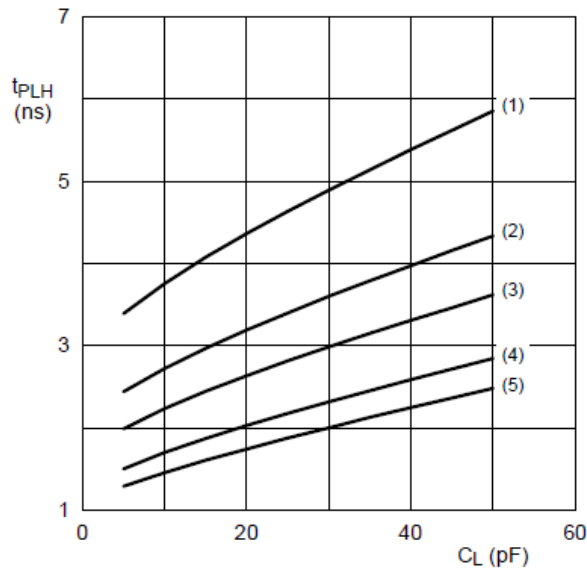


c. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 2.5V$
(1) $V_{CC(B)} = 1.2V$
(2) $V_{CC(B)} = 1.5V$
(3) $V_{CC(B)} = 1.8V$
(4) $V_{CC(B)} = 2.5V$
(5) $V_{CC(B)} = 3.3V$



d. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 2.5V$

Figure 8. Typical propagation delay versus load capacitance; $T_{amb} = 25^\circ C$



a. LOW to HIGH propagation delay (A to B);

V_{CC(A)}=3.3V

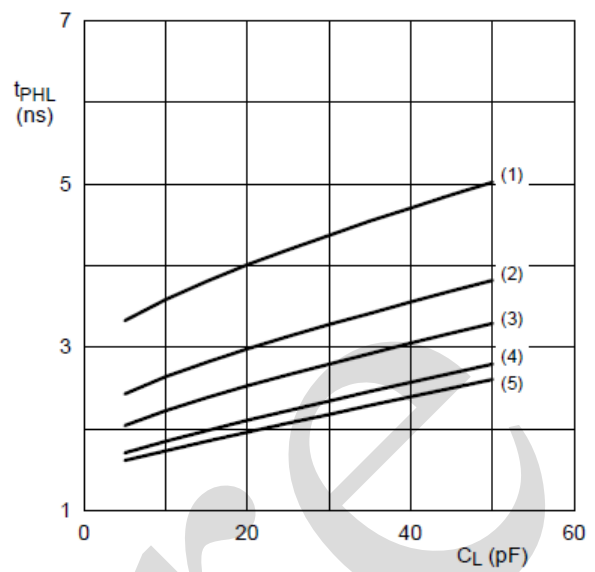
(1) V_{CC(B)}=1.2V

(2) V_{CC(B)}=1.5V

(3) V_{CC(B)}=1.8V

(4) V_{CC(B)}=2.5V

(5) V_{CC(B)}=3.3V



b. HIGH to LOW propagation delay (A to B);

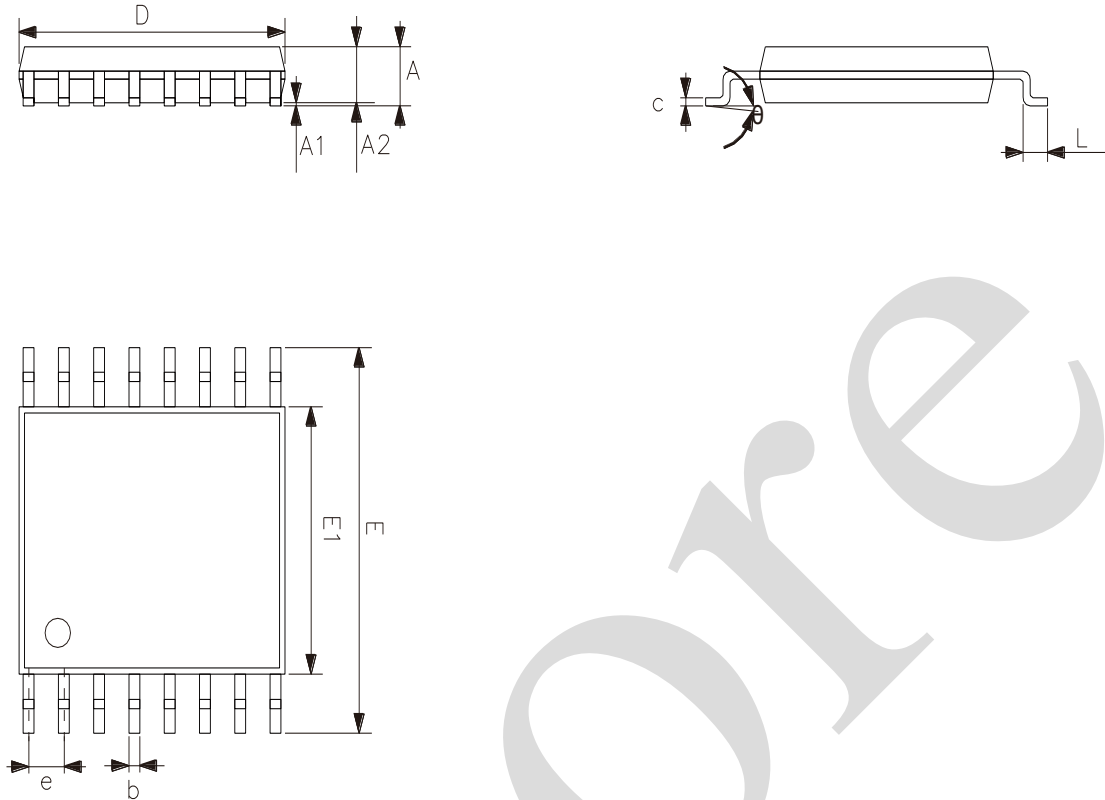
V_{CC(A)}=3.3V

Figure 9. Typical propagation delay versus load capacitance; T_{amb}=25°C



6、Package Information

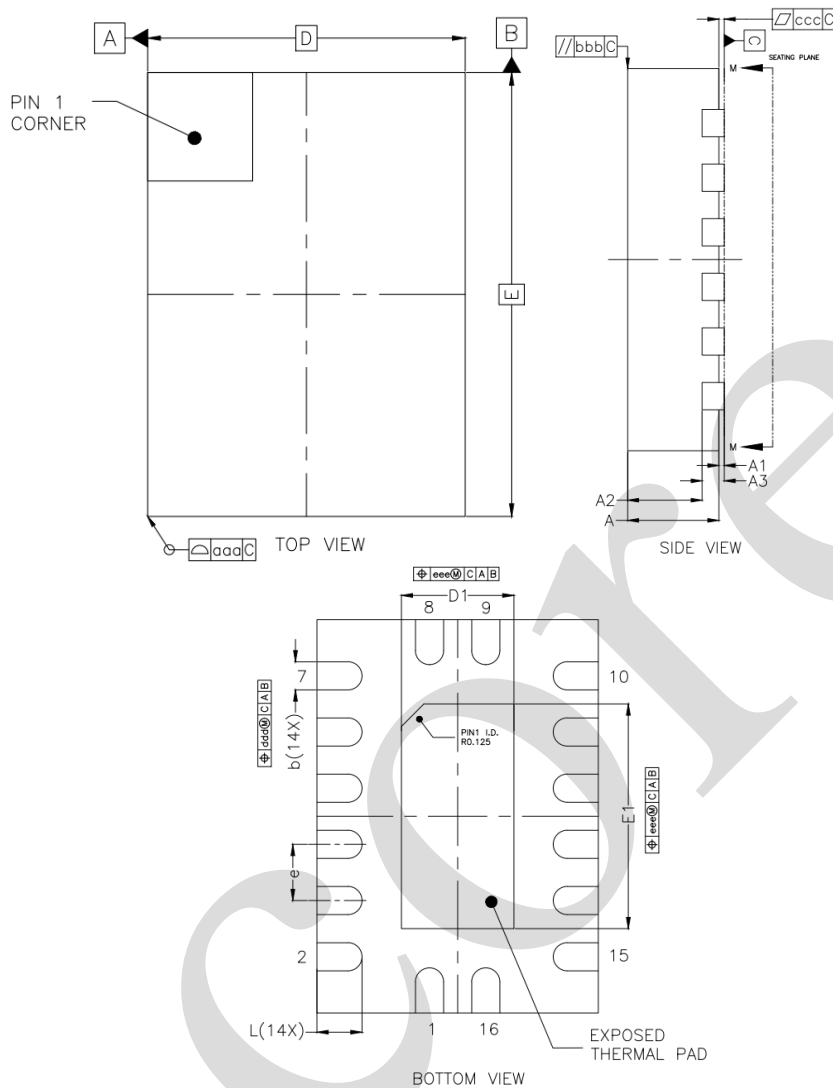
6.1、TSSOP16



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	—	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°



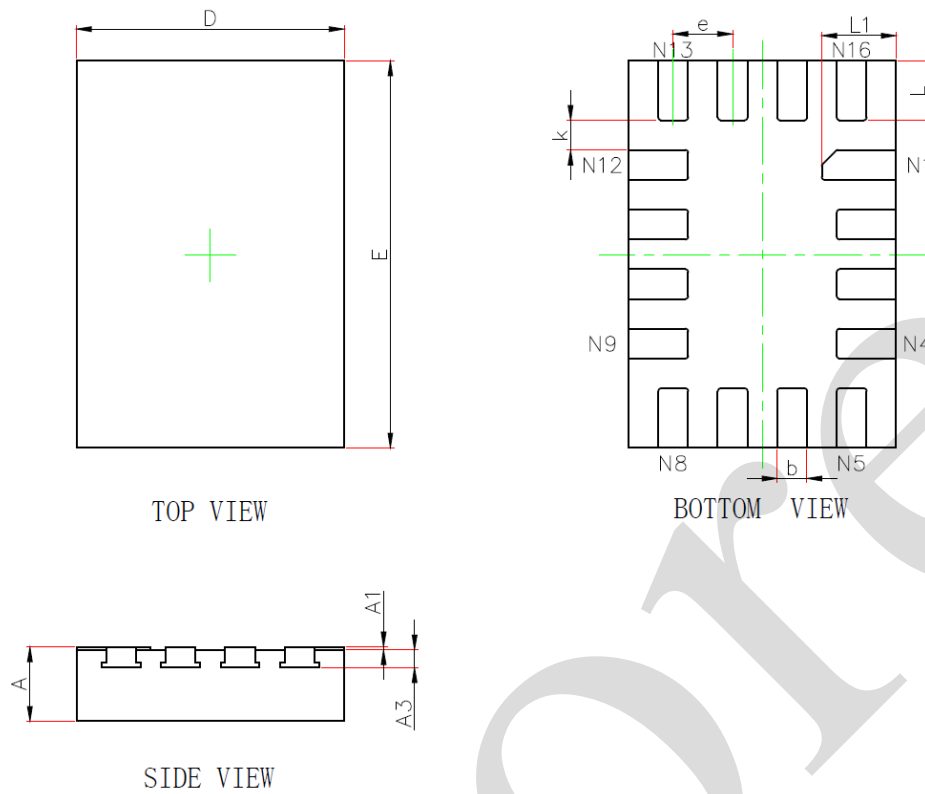
6.2、DHVQFN16



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.70
A3	0.20	
D	2.40	2.60
E	3.40	3.60
e	0.50	
b	0.18	0.30
L	0.30	0.50
D1	0.85	1.15
E1	1.85	2.15



6.3、MIS16



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	0.45	0.55
A1	0	0.046
A3	0.11	
D	1.75	1.85
E	2.55	2.65
k	0.15	
b	0.15	0.25
e	0.40	
L	0.35	0.45
L1	0.45	0.55



7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

We recommend you to read this chapter carefully before using this product.

The information in this chapter is provided for reference only and i-Core disclaims any express or implied warranties, including but not limited to applicability, special application or non-infringement of third party rights.

This product is not suitable for critical equipment such as life-saving, life-sustaining or safety equipment. It is also not suitable for applications that may result in personal injury, death, or serious property or environmental damage due to product malfunction or failure. I-Core will not be liable for any damages incurred by the customers at their own risk for such applications.

The customer is responsible for conducting all necessary tests i-Core's application to avoid failure in the application or the application of the customer's third party users. I-Core does not accept any liability.

The Company reserves the right to change or improve the information published in this chapter at any time. The information in this chapter are subject to change without notice. We recommend the customer to consult our sales staff before purchasing.

Please obtain related materials from i-Core's regular channels and we are not responsible for its content if it is provided by sources other than our company.

In case of any conflict between the Chinese and English version, the version is subject to the Chinese one.