AiP8563
I2C Real-Time Clock/Calendar Chip

Product Specification

Specification Revision History:

Version	Date	Description
2023-07-A1	2023-07	New
2023-07-A2	2023-07	Additional package
2023-11-A3	2023-11	Modify ordering information
2024-12-A4	2024-12	Modify the parameters
2026-01-A5	2026-01	Modify Ambient Temperature to -40~125℃

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1、General Description

AiP8563 is a low-power CMOS real-time clock/calendar chip, which provides a programmable clock output and an interrupt output. The address and data are transmitted serially through I^2C bus interface. The maximum bus speed is 400Kbits/s, and the embedded word address register will automatically increment after reading and writing data. It is widely used in mobile phones, portable instruments, fax machines and battery powered products.

Features:

- Low sleep current
- Programmable clock output frequency: 32.768KHz, 1024Hz, 32Hz and 1Hz
- Alarm and timing
- Built-in power reset function
- I^2C bus slave address: read, 0A3H； write, 0A2H
- Interrupt pin open-drain output
- Package information: DIP8/SOP8/TSSOP8/MSOP8

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Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP8563DA8.TB	DIP8	AiP8563	50 PCS/tube	40 tube/box	2000 PCS/box	Dimensions of plastic enclosure: 9.2mm×6.4mm Pin spacing: 2.54mm
AiP8563SA8.TB	SOP8	AiP8563	100 PCS/tube	100 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing: 1.27mm
AiP8563TA8.TB	TSSOP8	EPXX	100 PCS/tube	200 tube/box	20000 PCS/box	Dimensions of plastic enclosure: 3.0mm×3.0mm Pin spacing: 0.65mm
AiP8563TB8.TB	TSSOP8	8563	100 PCS/tube	200 tube/box	20000 PCS/box	Dimensions of plastic enclosure: 3.0mm×4.4mm Pin spacing: 0.65mm
AiP8563MA8.TB	MSOP8	AiP8563	100 PCS/tube	100 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 3.0mm×3.0mm Pin spacing: 0.65mm

Reel packing specifications:

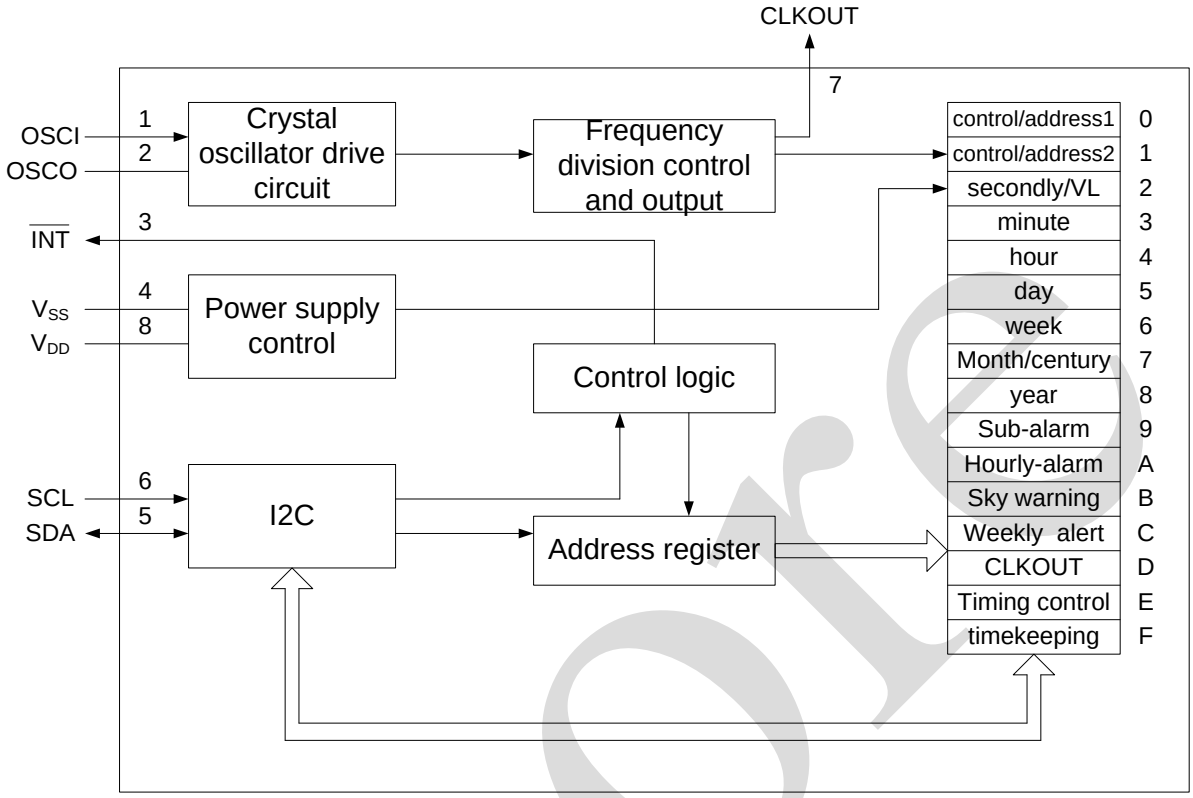
Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP8563SA8.TR	SOP8	AiP8563	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing: 1.27mm
AiP8563TA8.TR	TSSOP8	EPXX	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 3.0mm×3.0mm Pin spacing: 0.65mm
AiP8563TB8.TR	TSSOP8	8563	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 3.0mm×4.4mm Pin spacing: 0.65mm
AiP8563MA8.TR	MSOP8	AiP8563	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 3.0mm×3.0mm Pin spacing: 0.65mm

Note 1: “XX” refers to variable content, meaning package batch serial number.

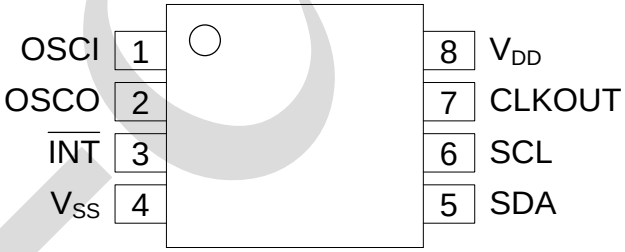
Note 2: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram



2.2、Pin Configurations



2.3、Pin Description

IO	Symbol	Description	IO	Symbol	Description
1	OSCI	Crystal Oscillator Input	5	SDA	Serial data I/O
2	OSCO	Crystal Oscillator Output	6	SCL	Serial clock input
3	/INT	Interrupt(open-drain: low enable)	7	CLKOUT	Clock output(open-drain)
4	V_{SS}	GND	8	V_{DD}	Power supply

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, unless otherwise specified)

Characteristic	Symbol	Conditions	Min.	Max.	Unit
Supply Voltage	V_{DD}	-	-0.5	+6.5	V
Supply Current	I_{DD}	-	-50	+50	mA
Input Voltage of SCL and SDA Input Pins	V_I	-	-0.5	+6.5	V
Output Voltage of OSCI Input Pin		-	-0.5	V_{DD}+0.5	V
Output Voltage of CLKOUT and /INT Output Pins	V_O	-	-0.5	+6.5	V
Power Dissipation	P_D	-	-	350	mW
Ambient Temperature	T_{amb}	-	-40	+125	℃
Storage Temperature	T_{stg}	-	-65	+150	℃
Lead Soldering Temperature	T_L	DIP	250		℃
		SOP/TSSOP/MSOP	260		℃

3.2、Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	1.8	5	5.5	V
High-Level Input Voltage	V_{IH}	0.7V_{DD}	-	V_{DD}	V
Low-Level Input Voltage	V_{IL}	V_{SS}	-	0.3V_{DD}	V

3.3、Electrical Characteristics

3.3.1、DC Characteristics

(T_{amb}=25℃, V_{DD}=1.8~5.5V, V_{SS}=0V; Fosc=32.768KHz; Crystal oscillator R_S=40KΩ; C_1=8pF, unless otherwise specified)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	I^2C bus disable	1.0	-	5.5	V
		I^2C bus enable, f_{SCL}=400KHz	1.8	-	5.5	V
Supply Current: CLOCKOUT Disable（FE=0）	I_{DD1}	f_{SCL}=400KHz	-	-	800	uA
		f_{SCL}=100KHz	-	-	200	uA
		f_{SCL}=0KHz，V_{DD}=2V	-	250	650	nA
		f_{SCL}=0KHz，V_{DD}=3V	-	270	700	nA
		f_{SCL}=0KHz，V_{DD}=5V	-	300	1000	nA
Supply Current: CLOCKOUT Enable $F_{CLOCKOUT}$=32KHz (FE=1)	I_{DD2}	f_{SCL}=0KHz，V_{DD}=2V	-	450	1450	nA
		f_{SCL}=0KHz，V_{DD}=3V	-	550	1500	nA
		f_{SCL}=0KHz，V_{DD}=5V	-	850	2000	nA
Low-Level Input Voltage	V_{IL}	-	V_{SS}	-	0.3V_{DD}	V
High-Level Input Voltage	V_{IH}	-	0.7V_{DD}	-	V_{DD}	V
Low-Level Output Current(SDA)	I_{OL}	V_{OL}=0.4V，V_{DD}=5V	3	-	-	mA
Low-Level Output	I_{OL}		1	-	-	mA

Current(/INT)						
Low-Level Output Current(CLKOUT)	I_{OL}		1	-	-	mA
Power-Low Detection Value	V_{LOW}	T_{amb}=25℃	-	1.0	-	V

3.3.2、AC Characteristics

(T_{amb}=25℃, V_{DD}=1.8~5.5V, V_{SS}=0V; Fosc=32.768KHz; Crystal oscillator R_S=40KΩ; C_1=8pF, unless otherwise specified)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Crystal Oscillator						
Load Capacitance	C_L	-	10	20	35	pF
Quartz Crystal Oscillator Parameter（Fosc=32.768KHz）						
Serial Resistance	R_S	-	-	-	40	KΩ
Parallel Capacitance	C_L	-	-	10	-	pF
Adjustable Capacitance	C_T	-	5	-	25	pF
CLKOUT Output						
CLKOUT Duty Cycle	δ_{CLKOUT}	-	-	50	-	%
I²C Bus Timing Characteristics						
SCL Clock Frequency	f_{SCL}	-	-	-	400	KHz
START Condition Hold Time	$T_{HD;STA}$	-	0.6	-	-	us
Set-up Time for a Repeated START Condition	$T_{SU;STA}$	-	0.6	-	-	us
SCL LOW Time	T_{LOW}	-	1.3	-	-	us
SCL HIGH Time	T_{HIGH}	-	0.6	-	-	us
SCL and SDA Rise Time	T_R	-	-	-	0.3	us
SCL and SDA Fall Time	T_F	-	-	-	0.3	us
Capacitive bus line load	C_b	-	-	-	400	pF
Data Set-Up Time	$T_{SU;DAT}$	-	100	-	-	ns
Data Hold Time	$T_{HD;DAT}$	-	0	-	-	ns
Set-up Time for STOP Condition	$T_{SU;STO}$	-	4.0	-	-	us

Note: The access time of I²C bus must be less than one second under the conditions of two START conditions or one START and STOP condition.

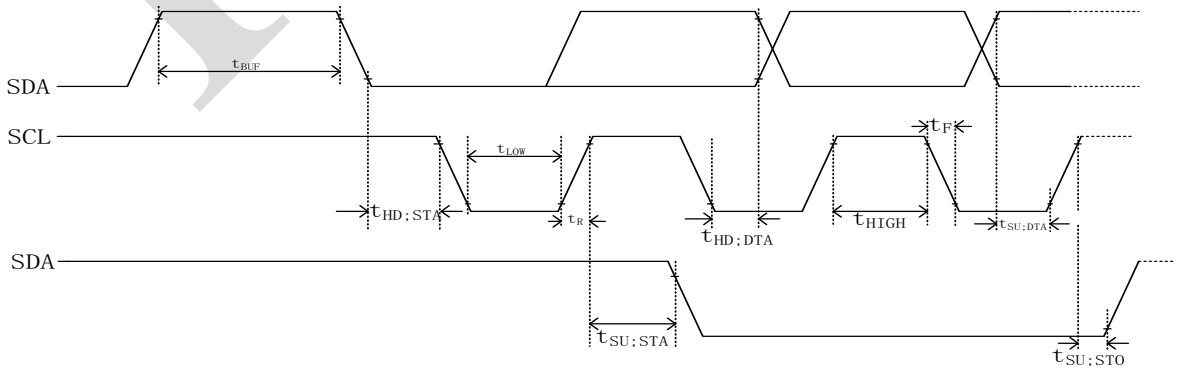


Figure 3. I²C Timing Waveform

4、Function Introduction

AiP8563 contains 16 sets of 8-bit registers. Address 00H～01H is used for control register and status register, address 02H～08H is used for clock counter, address 09H～0CH is used for alarm register, address 0DH controls the output frequency of CLKOUT pin, and addresses 0EH and 0FH are used for timer control register and timer register respectively.

Except for week and week alarm registers, the encoding format of second, minute, hour, day, month, year, minute alarm, hour alarm and day alarm registers is BCD.

4.1、Alarm Function Mode

When the AE bit in the alarm register is cleared to 0, the corresponding alarm is valid. The alarm will be generated every minute to every week. Setting the alarm flag bit AF is used to generate an interrupt, and AF can only be cleared by software.

4.2、Timer

The down counter (address 0FH) is controlled by the timer control register (address 0EH), which is used to set the frequency of the timer control register(4096, 64, 1, or 1/60Hz) and whether the timer is valid or not. The timer counts down from the set value. At the end of each countdown, the timer sets the flag bit TF, which can only be cleared by software and is used to generate an interrupt signal. TI/TP controls the conditions for interrupt generation. When reading the timer, the current countdown value is returned.

4.3、CLKOUT Output

CLKOUT outputs a programmable square wave, and the frequency of the square wave is selected by the CLKOUT frequency register: 32.768KHz (default), 1024Hz, 32Hz and 1Hz. CLKOUT is an open-drain output, which is connected to the power supply when used, otherwise it is high impedance.

4.4、Reset

AiP8563 includes a built-in reset circuit, which starts to operate when the crystal oscillator circuit stops operating. In the reset state, I^2C bus is initialized, registers TF, VL, TD1, TD0, TESTC and AE are set to logic 1, and other registers and address pointers are cleared to 0.

4.5、Power-Down Detector and Clock Monitor

AiP8563 contains power-down detection. When V_{DD} is lower than V_{low}, bit VL is set to 1, indicating that an inaccurate clock/calendar may be generated, and the VL flag bit can only be cleared by software.

4.6、Register Description

Note: "—" indicates the invalid bit, "0" indicates the bit logic is 0.

Address	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H	Control/status register 1	TEST	0	STOP	0	TEST C	0	0	0
01H	Control/status register 2	0	0	0	TI/TP	AF	TF	AIE	TIE
02h	Second	VL	00～59BCD code format number						
03h	Minute	—	00～59BCD code format number						
04h	Hour	—	—	00～23BCD code format number					
05h	Day	—	—	01～31BCD code format number					
06h	Week	—	—	—	—	—	0~6		
07h	Month/century	C	—	—	01～12BCD code format number				
08h	Year	00～99BCD code format number							
09h	Minute alarm	AE	00～59BCD code format number						
0Ah	Hour alarm	AE	—	00～23BCD code format number					
0Bh	Day alarm	AE	—	01～31BCD code format number					
0Ch	Week alarm	AE	—	—	—	—	0~6		
0DH	CLKOUT frequency register	FE	—	—	—	—	—	FD1	FD0
0EH	Timer Control register	TE	—	—	—	—	—	TD1	TD0
0FH	Timer countdown value register	Timer countdown value							

4.6.1、Control/State Register 1（Address 00H）

Bit	Symbol	Description
7	TEST1	TEST1=0：normal mode TEST1=1：test mode
5	STOP	STOP=0：the clock operates STOP=1：all the frequency dividers are set to logic 0; The clock stops operating
3	TESTC	TESTC=0：power reset function fails (logic 0 is set in normal mode) TESTC=1：the power reset function is valid
6,4,2,1,0	0	The default value is set to logic 0

4.6.2、Control/State Register 2（Address 01H）

Bit	Symbol	Description
7,6,5	0	The default value is set to logic 0
4	TI/TF	TI/TP=0: INT is valid when TF is valid (depending on the state of TIE) TI/TP=1：INT pulse is valid (depending on the state of TIE) Note: If both AF and AIE are valid, INT is always valid.
3	AF	When the alarm occurs, AF is set to logic 1; When the timer countdown stops, TF is set to logic 1; If both timer and alarm interrupt are requested, the interrupt source is determined by AF and TF. If one flag bit is cleared to prevent another flag bit from being rewritten, the logic instruction AND should be applied.
2	TF	

1	AIE	AIE=0: The alarm interrupt is invalid; AIE=1: The alarm interrupt is valid
0	TIE	AIE=0: The timer interrupt is invalid; AIE=1: The timer interrupt is valid

/INT operation (bit TI/TP=1）

Source Clock(Hz)	/INT Cycle	
	n=1	n>1
4096	1/8192	1/4096
64	1/128	1/64
1	1/64	1/64
1/60	1/64	1/64

Note 1: n is the value of the countdown timer. When n=0, the timer stops operating.

AF and TF value description

R/W	Bit: AF		Bit: TF	
	Value	Description	Value	Description
Read	0	The alarm flag is invalid	0	The timer flag is invalid
	1	The alarm flag is valid	1	The timer flag is valid
Write	0	The alarm flag is cleared	0	The timer flag is cleared
	1	The alarm flag remains unchanged	1	The timer flag remains unchanged

4.6.3、Second Register（Address 02H）

Bit	Symbol	Description
7	VL	VL=0：Ensure accurate clock/calendar data VL=1：Not ensure accurate clock/calendar data
6～0	<second>	Second in BCD format, values are 00 ~ 59. For example: < second > = 1011001, representing 59 seconds.

4.6.4、Minute Register（Address 03H）

Bit	Symbol	Description
7	—	Invalid bit
6～0	<minute>	Minute in BCD format, values are 00～59

4.6.5、Hour Register（Address 04H）

Bit	Symbol	Description
7～6	—	Invalid bit
5～0	<hour>	Hour in BCD format, values are 00～23

4.6.6、Day Register（Address 05H）

Bit	Symbol	Description
7～6	—	Invalid bit
5～0	<day>	Day in BCD format, values are 01～31 In leap year, AiP8563 automatically adds a value to February, making it 29 days.

4.6.7、Day Register Bit Description（Address 06H）

Bit	Symbol	Description
7～3	—	Invalid
2～0	<week>	Weeks value 0～6

The week setting is as follows:

Day	Bit2	Bit1	Bit0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

4.6.8、Month/Century Register（Address 07H）

Bit	Symbol	Description
7	C	Century position; C=0 specifies that the number of centuries is 20××; C=1 specifies that the number of centuries is 19××. When the xx in the register changes from 99 to 00, the century bit will change.
6～5	—	Invalid bit
4～0	<month>	Month in BCD format, values are 01～12

The month setting is as follows：

Month	Bit4	Bit3	Bit2	Bit1	Bit0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

4.6.9、Year Register(Address 08H)

Bit	Symbol	Description
7～0	<year>	Year in BCD format, values are 00～99

4.6.10、Minute Alarm Register（Address 09H）

Bit	Symbol	Description
7	AE	AE=0, minute alarm is valid; AE=1, minute alarm is invalid
6～0	<minute alarm>	Minute alarm in BCD format, values are 00～59

4.6.11、Hour Alarm Register（Address 0AH）

Bit	Symbol	Description
7AE	AE	AE=0, hour alarm is valid; AE=1, hour alarm is invalid
6～0	<hour alarm>	Hour alarm in BCD format, values are 00～23

4.6.12、Day Alarm Register（Address 0BH）

Bit	Symbol	Description
7	AE	AE=0, day alarm is valid; AE=1, day alarm is invalid
6～0	<day alarm>	Day alarm in BCD format, values are 00～31

4.6.13、Week Alarm Register（Address 0CH）

Bit	Symbol	Description
7	AE	AE=0, week alarm is valid; AE=1, week alarm is invalid
6～0	<week alarm>	Week alarm in BCD format, values are 0～6

4.6.14、CLKOUT Frequency Register（Address 0DH）

Bit	Symbol	Description
7	FE	FE=0, CLKOUT has no output, showing high-impedance FE=1, CLKOUT output is valid
6～2	—	Invalid bit
1	FD1	Set the output frequency of CLKOUT
0	FD0	

CLKOUT frequency setting is as follows:

FD1	FD0	f_{CLKOUT}
0	0	32.768KHz
0	1	1024Hz
1	0	32Hz
1	1	1Hz

4.6.15、Countdown Timer Register（Address 0EH）

Bit	Symbol	Description
7	TE	TE=0, timer is invalid; TE=1, timer is valid
6～2	—	Invalid bit
1	TD1	The timer clock frequency selection bit determines the clock frequency of the countdown timer. When not in use, TD1 and TD0 should be set to “11” (1/60hz) to reduce power consumption.
0	TD0	

Timer clock frequency setting is set as follow:

TD1	TD0	Timer clock frequency（Hz）
0	0	4096
0	1	64
1	0	1
1	1	1/60

4.6.16、Timer Countdown Value Register（Address 0FH）

Bit	Symbol	Description
7～0	<Timer Countdown Value>	Countdown value “n” Countdown period = n/clock frequency

4.7、EXT_CLK Test Mode

The test mode is used for online testing, establishing the test mode and controlling the operation of RTC. The test mode is set by bit TEST1 of control/state register 1. In the test mode, instead of the 64Hz frequency signal in the chip, the frequency input by CLKOUT will generate a time increment of 1 second every 64 rising edges.

4.8、POR Failure Mode

The reset time of POR is related to the starting time of the crystal oscillator. AiP8563 has a built-in POR failure circuit, which can save the test time. The failure timing of POR is shown in the following figure, in which the time is the minimum required.

When entering the failure mode, the chip immediately stops resetting, and the operation enters the EXT__CLK test mode through I^2C bus. Setting TESTC logic 0 can eliminate the failure mode, and setting TESTC as logic 1 can re-enter the failure mode.

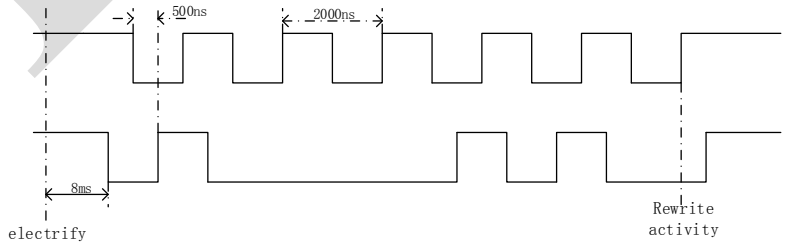


Figure 4. POR Failure Timing

4.9、Serial Interface

The serial interface of AiP8563 is I^2C bus.

4.9.1、START and STOP Timing

It is the START timing when the data line is on the falling edge and the clock line is high. and it is the STOP timing when the the data line is on the rising edge and the clock line is high.

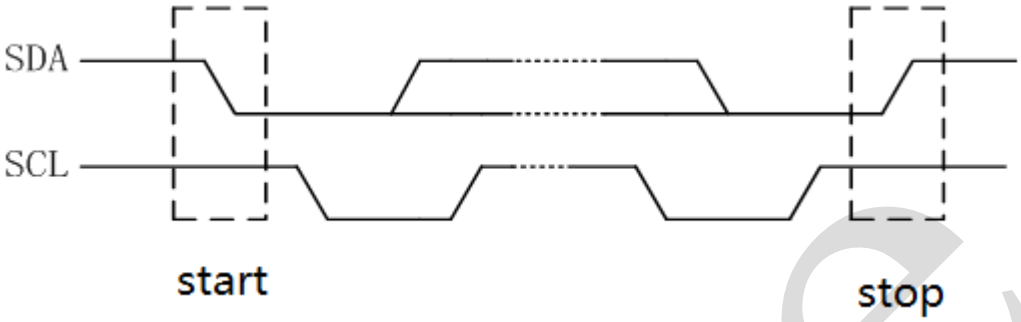


Figure 5. START and STOP Timing of I²C Bus

4.9.2、Bit Transmission

Each clock pulse transmits a data bit, and the data on the SDA line should remain stable when the clock pulse is high.

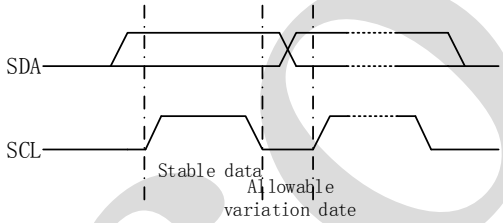


Figure 6. Transmission Bit of I²C Bus

4.9.3、Flag Bit

Multi-bit data can be transmitted between START and STOP timing. A flag bit is added after each 8-bit byte, and the transmitter generates a high-level flag bit. At this time, the master device generates a flag clock pulse.

The slave receiver must generate a flag bit after receiving each byte, and the master receiver must also generate a flag bit after receiving each byte transmitted from the transmitter. When the flag bit clock pulse appears, the SDA line should be kept low (starting and holding time should be considered). The transmitter should be low when the slave device receives the last byte, so that the receiver can generate a flag bit. At this time, the master device can generate a STOP timing.

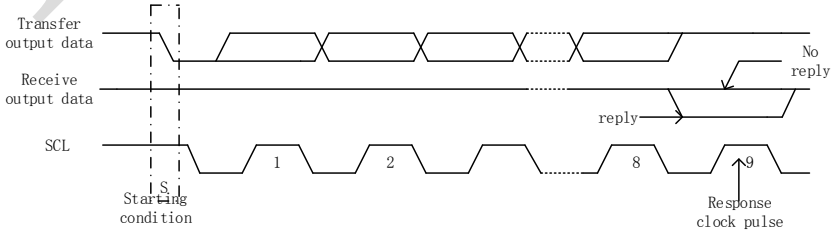


Figure 7. Flag Bits I²C of I²C Bus

4.9.4、 I²C Bus Protocol

Before transmitting data through I²C bus, the receiving device should indicate the address, and this address will be transmitted together with the first transmission byte after I²C bus is started. AiP8563 can be applied as a slave receiver or a slave transmitter. At this time, the clock signal line SCL can only be an input signal line, and the data signal line SDA is a bidirectional signal line.

See the figure below for the slave address of AiP8563.

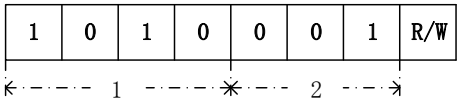


Figure 8. Slave Address

Clock/calendar chip read/write cycle: the configuration of I2C bus in three AiP8563 read/write cycles is shown in the following three figures, in which the lower four bits of the word address are applied to indicate the accessed register, and the upper four bits of the word address are not applied.

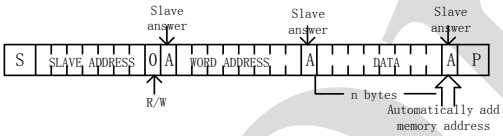


Figure 9.Master transmitter to slave receiver(write mode)

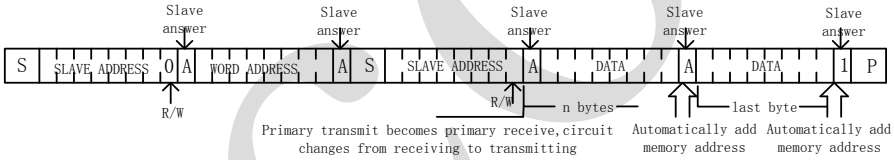


Figure 10. The master device reads the data after setting the word address(writing address: read data)

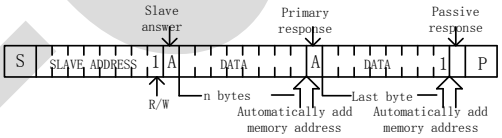
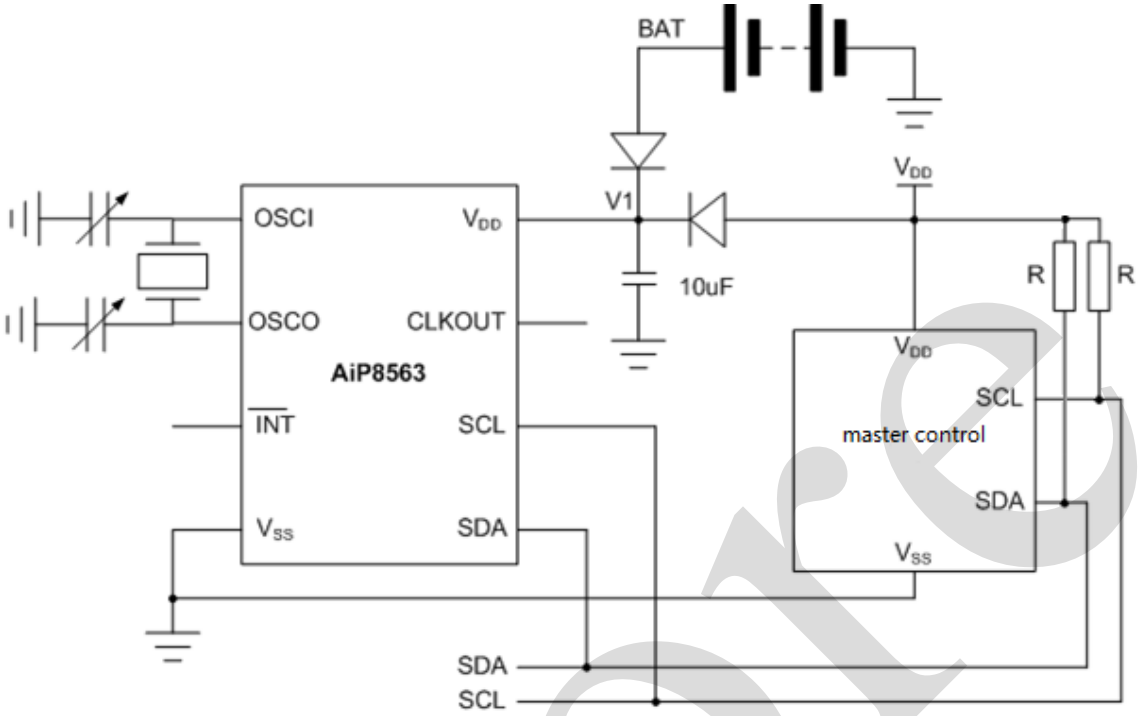


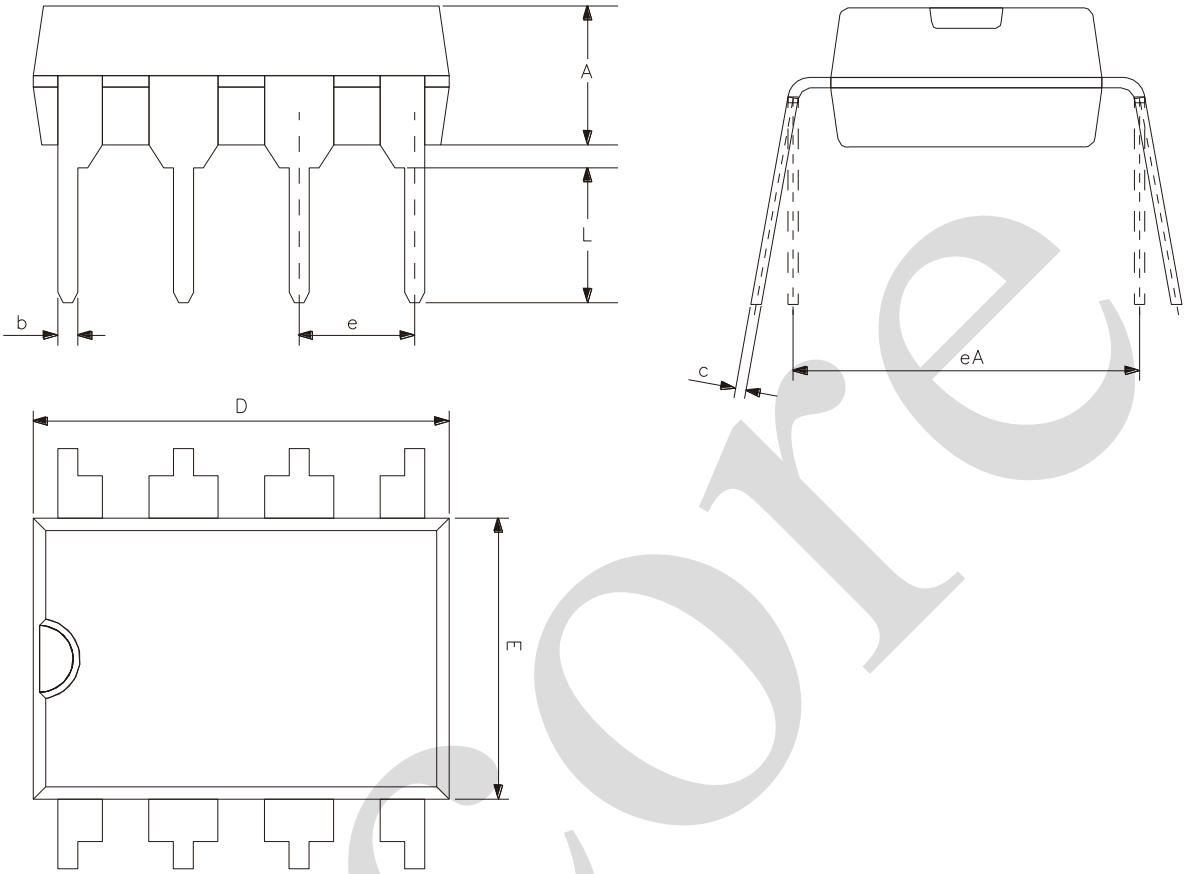
Figure 11. The master device reads the data followed by the first byte data of the slave device (read mode)

5、Typical Application Circuit



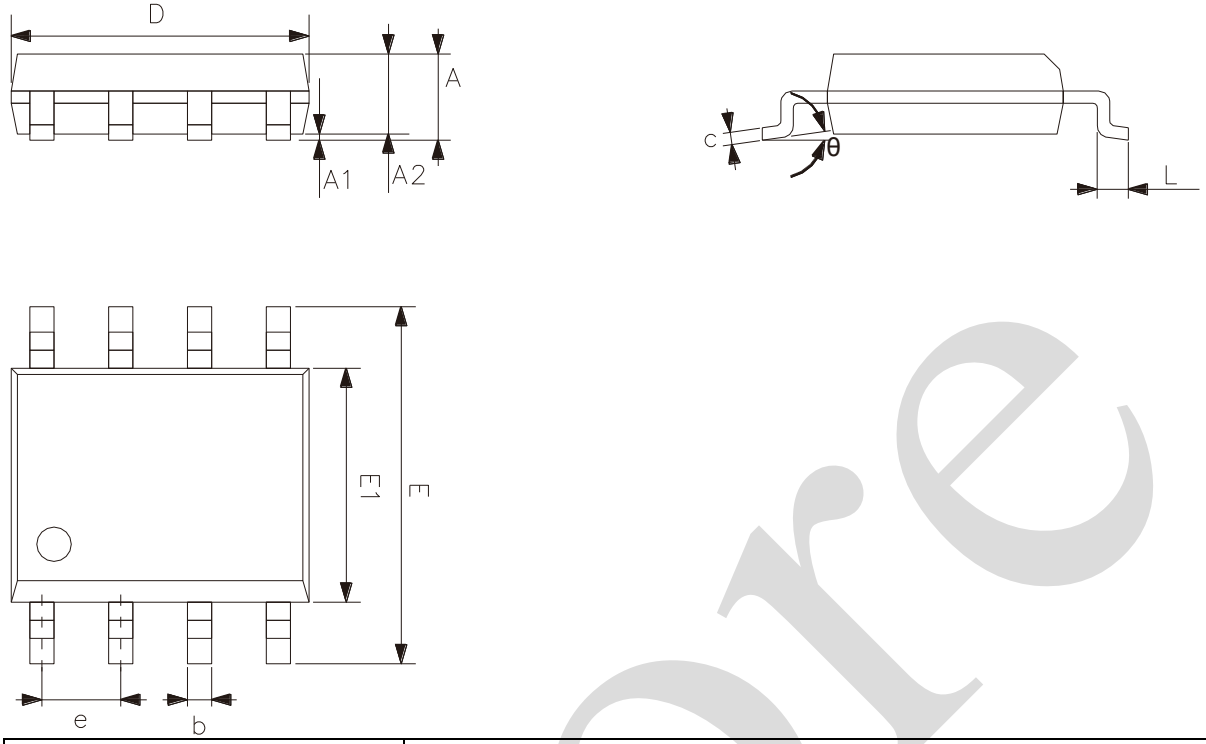
6、Package Information

6.1、DIP8



Symbol	Size（mm）	
	Min.	Max.
A	3.00	3.60
b	0.36	0.56
c	0.20	0.36
D	9.00	9.45
E	6.15	6.60
e	2.54	
eA	7.62	9.30
L	3.00	—

6.2、SOP8



Symbol	Size（mm）	
	Min.	Max.
A	1.35	1.80
A1	0.05	0.25
A2	1.25	1.55
D	4.70	5.10
E	5.80	6.30
E1	3.70	4.10
b	0.306	0.51
c	0.19	0.25
e	1.27	
L	0.40	0.89
θ	0°	8°

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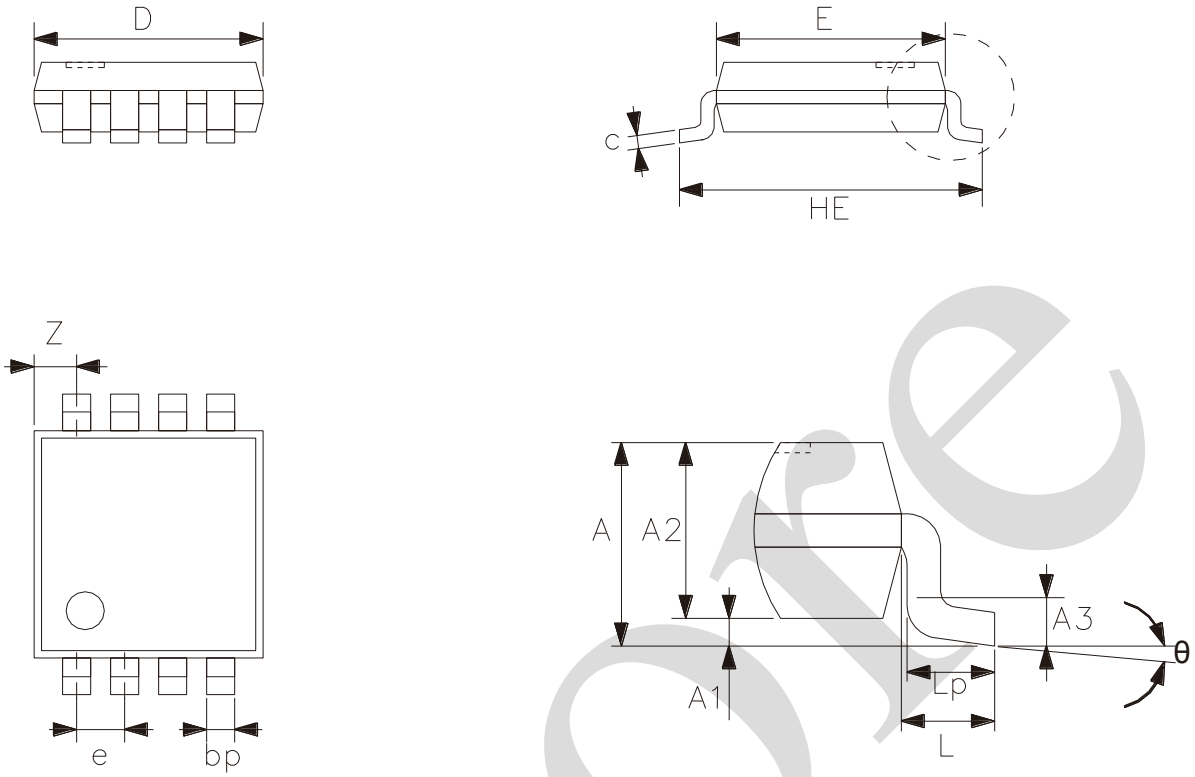
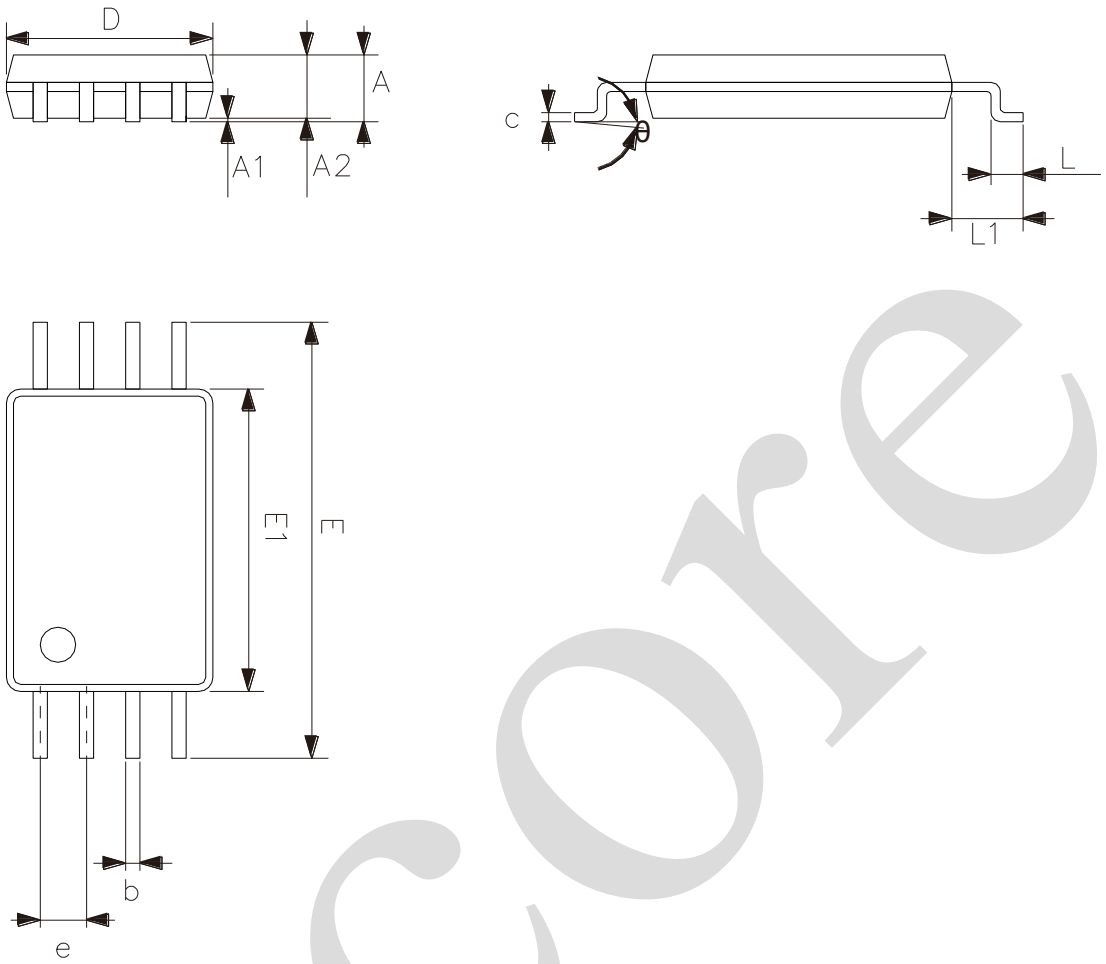
6.3、TSSOP8(3*3)



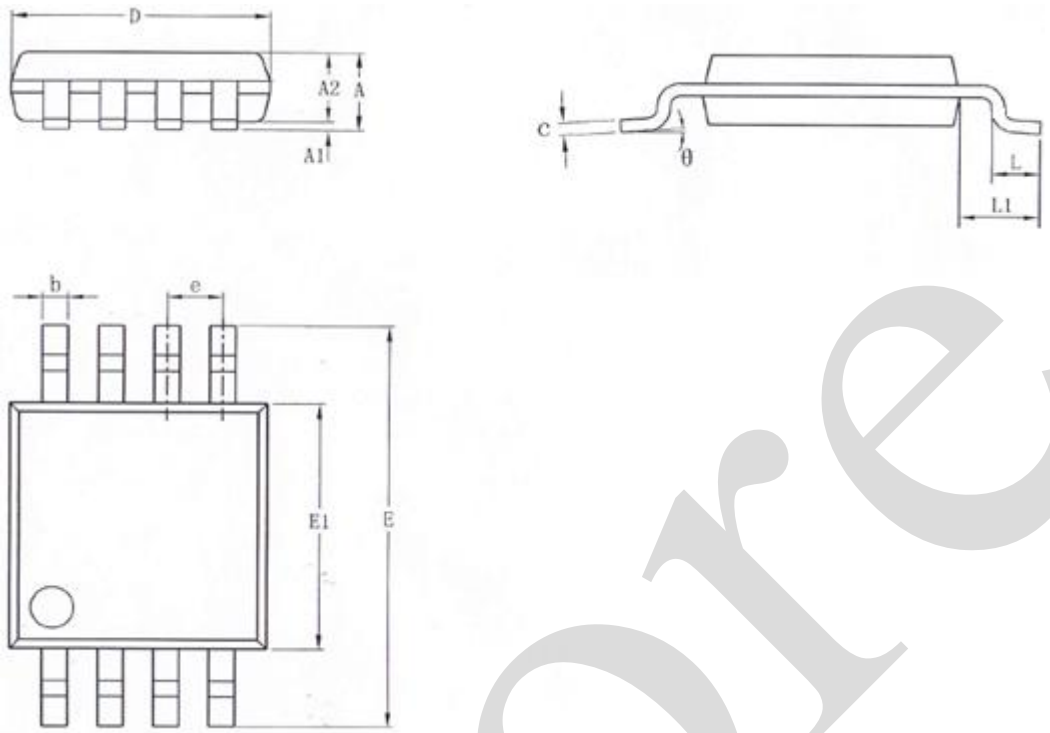
Symbol	Size（mm）	
	Min.	Max.
A	—	1.10
A1	0	0.15
A2	0.75	0.95
A3	0.25	
bp	0.22	0.38
C	0.08	0.18
D	2.90	3.10
E	2.90	3.10
HE	3.90	4.10
L	0.50	
Lp	0.33	0.47
e	0.65	
Z	0.35	0.70
θ	0°	8°

6.4、TSSOP8(3*4.4)



Symbol	Size（mm）	
	Min	Max
A	—	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

6.5、MSOP8



Symbol	Size（mm）	
	Min.	Max.
A	—	1.10
A1	0.05	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.90	3.10
E	4.70	5.10
E1	2.90	3.10
e	0.65	
L	0.40	0.80
L1	0.95	
θ	0°	8°

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

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