



BU9792

36 Seg × 4 Com Low Power LCD

Drivers and Controllers

Product Specification

Specification Revision History:

Version	Date	Description
2011-12-A1	2011-12	New
2025-08-B1	2025-08	Modify ambient temperature



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1、 General Description

BU9792 is a general-purpose single-chip LCD driver circuit capable of driving 144-segment characters or graphics. It is compatible with most microprocessors/microcontrollers and communicates via a two-wire bus. It is mainly used to drive segment-type LCD displays.

Features:

- Operating voltage: 2.5V to 5.5V
- LCD driver outputs: 4 Common lines, 36 Segment lines
- Built-in display RAM capacity: $36 \times 4 = 144$ bits
- Two-wire bus interface (SCL, SDA)
- Built-in oscillation circuit
- Built-in LCD driver circuit: 1/4 duty, with optional 1/2 and 1/3 bias
- Built-in Buffer AMP
- Low-power design
- Built-in wait mode
- Built-in power-on reset circuit
- Built-in blinking function
- Package Information: LQFP48/TSSOP48

**Ordering Information:****Tube packing specifications:**

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
BU9792AFUV	TSSOP48	BU9792AFUV	38 PCS/tube	100 tube/box	3800 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin Spacing: 0.5mm
BU9792AFUV LA48.TB	LQFP48	BU9792AFUV	250 PCS/plate	10 plate/box	2500 PCS/box	Dimensions of plastic enclosure: 7.0mm×7.0mm Pin Spacing: 0.5mm

Reel packing specifications:

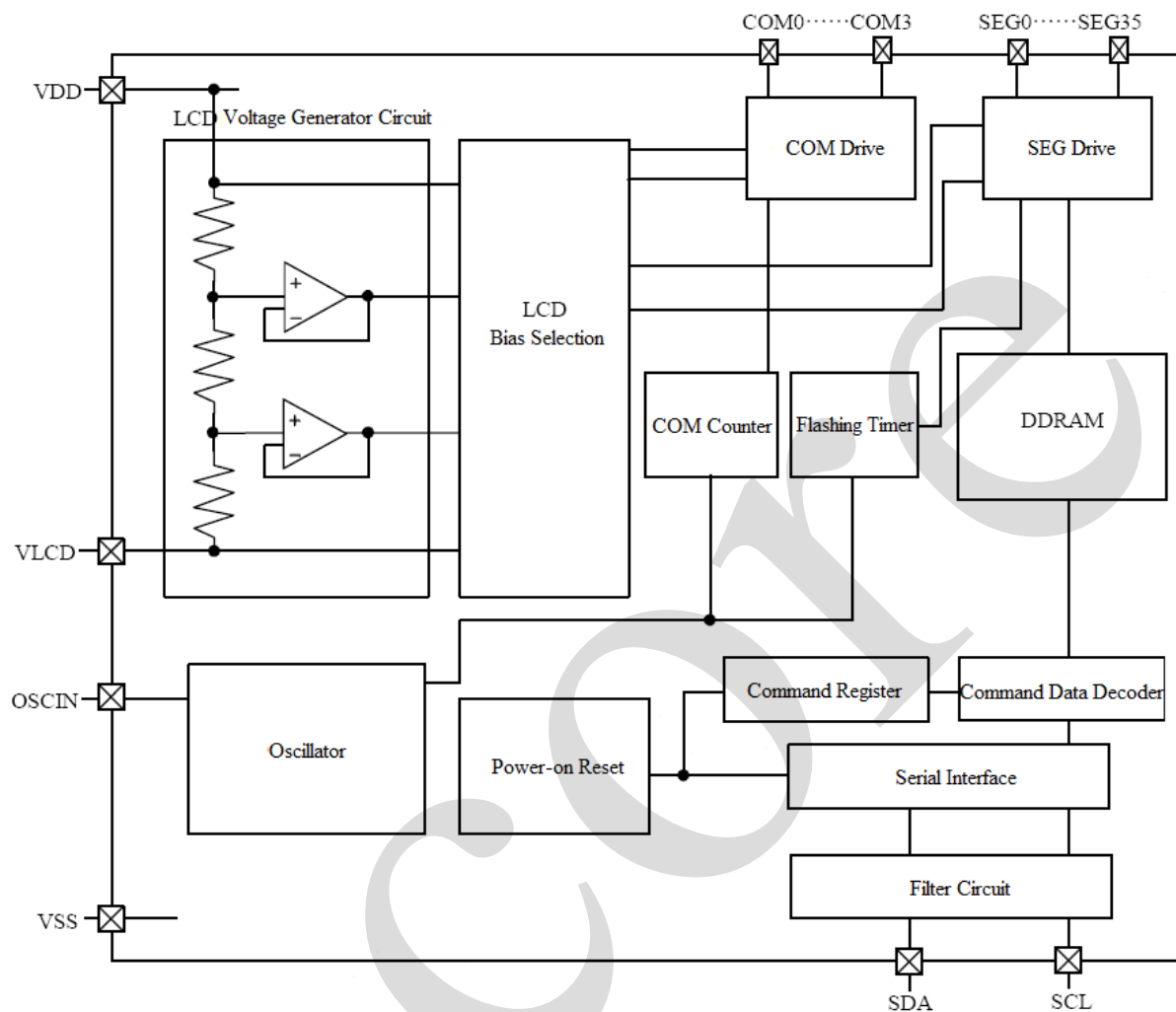
Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
BU9792AFUV	TSSOP48	BU9792AFUV	2000 PCS/reel	2000 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin Spacing: 0.5mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



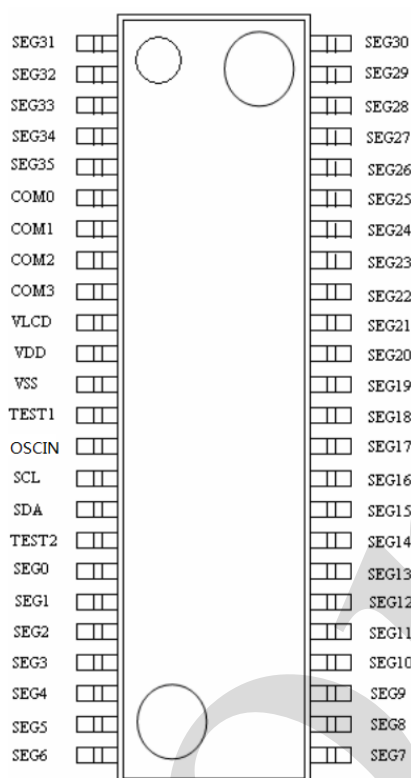
2、Block Diagram And Pin Description

2.1、Block Diagram

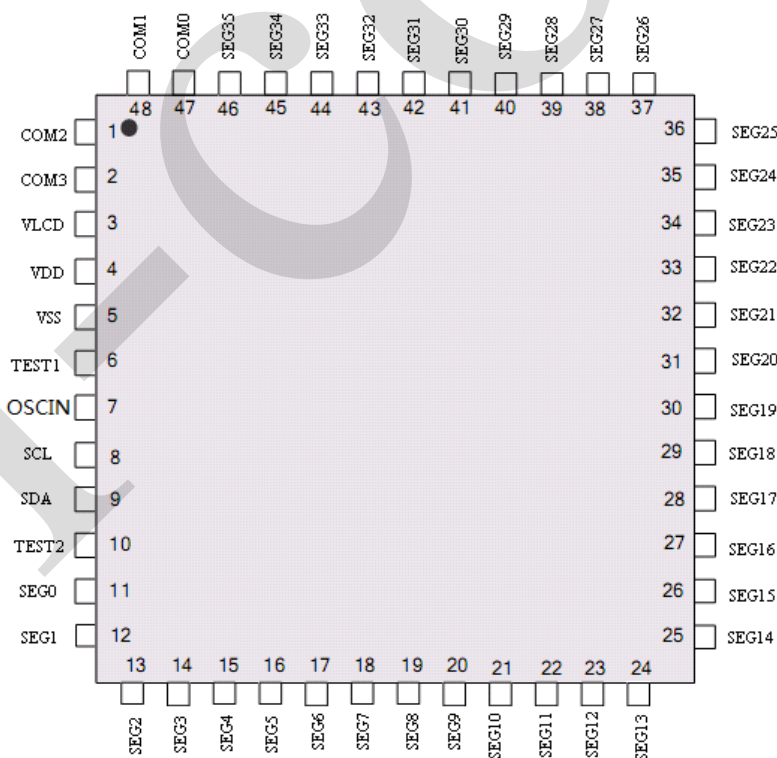




2.2、Pin Configurations



TSSOP48



LQFP48



2.3、Pin Description

Pin No.		Symbol	Description	Block Diagram
TSSOP48	LQFP48			
1~5	42~46	SEG31~SEG35	Output (Segment): LCD Segment Output	—
6~9	47~48 1~2	COM0~COM3	Output(Common): LCD Common Output	—
10	3	VLCD	LCD Voltage Input: LCD Driving Voltage Input	
11	4	VDD	Logic power supply	
12	5	VSS	Logic Ground, connected to system ground	
13	6	TEST1	Test Pin 1: Test input pin. Short to VSS.	
14	7	OSCIN	External Clock Input: External clock / internal clock selection is configured via register command. Short to VSS when using internal oscillator circuit.	
15	8	SCL	Clock Pin : Two-wire serial clock input	
16	9	SDA	Data Pin: Two-wire serial data input	
17	10	TEST2	Test Pin 2: POR enable pin. H: POR disabled (use Software Reset) L: POR enabled	
18~48	11~41	SEG0~SEG30	Output (Segment): LCD Segment Drive Output	-



3、Electrical Parameter

3.1、Absolute Maximum Ratings

($T_{amb}=25^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Conditions	Ratings	Unit
supply voltage	VDD	-	-0.5~+7.0	V
LCD voltage	VLCD	-	-0.5~VDD	V
power dissipation	P_D	-	0.64	W
ambient temperature	T_{amb}	-	-40~+105	$^{\circ}\text{C}$
storage temperature	T_{stg}	-	-55~+125	$^{\circ}\text{C}$
Soldering temperature	T_L	10s	260	$^{\circ}\text{C}$

Note: Above 25°C , the rated power dissipation decreases by 6.4mW per degree Celsius temperature rise.

3.2、Recommended Operating Conditions

($T_{amb}=25^{\circ}\text{C}$, VSS=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
supply voltage	VDD	2.5	-	5.5	V
LCD voltage	VLCD	0	-	VDD-2.4	V

Note: VDD-VLCD $\geq$ 2.5V.

3.3、Electrical Characteristics

3.3.1、DC Characteristics

($T_{amb}=-40$ to $+105^{\circ}\text{C}$, VDD=2.5V to 5.5V, VSS=0V, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Static Current	I_{DDQ}	Display OFF, Oscillator OFF	-	-	5	μA
Operating Current	I_{DD}	-	-	7.5	20	μA
HIGH-level input voltage	V_{IH}	-	0.7VDD	-	VDD	V
Low-level input voltage	V_{IL}	-	VSS	-	0.3VDD	V
HIGH-level input current	I_{IH}	-	-	-	1	μA
Low-level input current	I_{IL}	-	-1	-	-	μA
SEG Output On-Resistance	SEG	R_{ON1}	$I_{load}=\pm 10\mu\text{A}$	-	3	$k\Omega$
	COM	R_{ON2}		-	3	$k\Omega$
VLCD Driving Voltage	V_O	VDD-VLCD $\geq$ 2.5V	0	-	VDD-2.4	V



3.3.2、AC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
oscillator frequency	f_{CLK}	-	56	80	104	Hz
input signal rise time	t_r	-	-	-	0.3	us
input signal fall time	t_f	-	-	-	0.3	us
SCL clock period	t_{CYC}	-	2.5	-	-	us
SCL high period	t_{HW}	-	0.6	-	-	us
SCL low period	t_{LW}	-	1.3	-	-	us
SDA setup time	t_{SDS}	-	100	-	-	ns
SDA hold time	t_{SDH}	-	100	-	-	ns
bus free time	t_{BUF}	-	1.3	-	-	us
START hold time	$t_{HD;STA}$	-	0.6	-	-	us
START setup time	$t_{SU;STA}$	-	0.6	-	-	us
STOP setup time	$t_{SU;STO}$	-	0.6	-	-	us

4、Testing Circuit

4.1、AC Testing Circuit

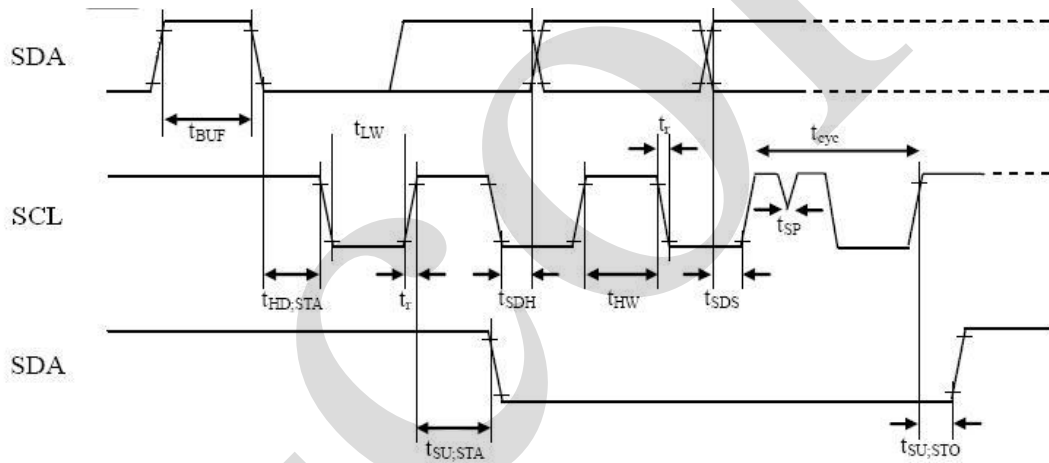


Figure 1. Two-wire interface AC characteristics diagram



4.2、Power-Up Considerations for BU9792

During power-up of the BU9792, both internal circuits and reset circuits (RESET), may temporarily operate in an unstable low-voltage region. As the VDD voltage ramps up, may cause malfunctions of incomplete reset states (RESET) during power-up initialization. To prevent such occurrences, the device incorporates: POR Circuit and Software Reset Functionality (RESET).To ensure proper internal reset initialization (RESET), the following conditions must be met during power-up:

- 1、 For POR operation, t_R , t_F , t_{OFF} , V_{bot} must satisfy recommended conditions:

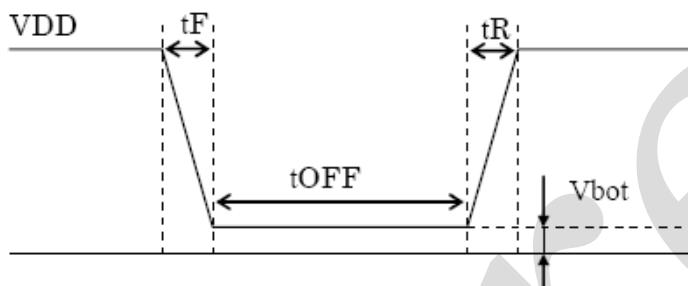


Figure 2. Rising edge waveform diagram

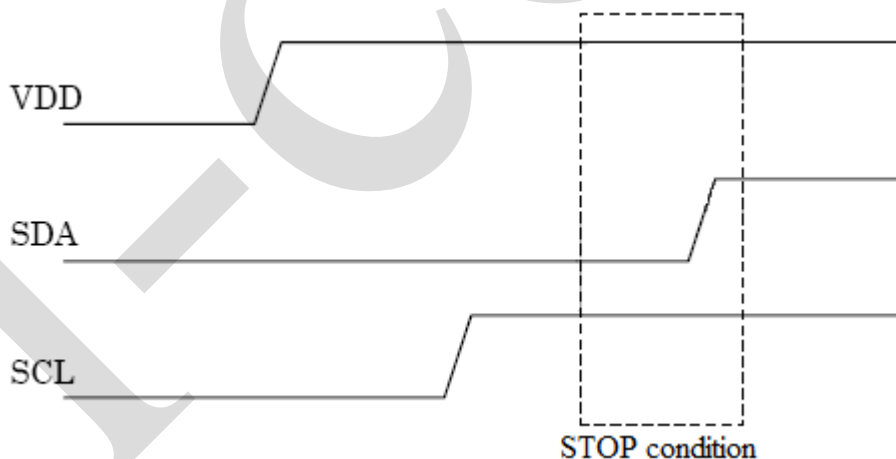
Recommended conditions for t_R , t_F , t_{OFF} , V_{bot} :

t_R	t_F	t_{OFF}	V_{bot}
1ms	1ms	100ms	Below 0.1V

Note: To enable POR function, the TEST2 pin must be pulled L.

- 2、 If POR circuit is inactive, execute the following post after the power-up:

- (1) Initiate STOP command when Two-Wire communication starts
- (2) Issue Software Reset via ICSET command



Note: POR circuit is disabled when TEST2 pin is set HIGH.

Command1: Key Read Command.

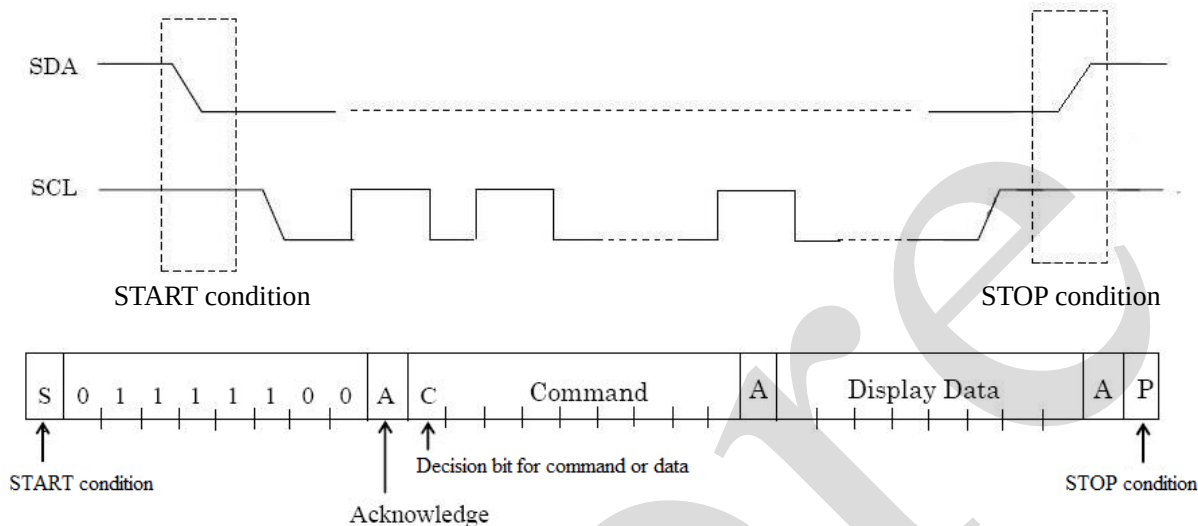
Data1~4: Key Value Data.



5、Function Description

5.1、Two-Wire Interface Communication

The BU9792 transfers data via a two-wire serial interface. Command input and data input through this I/F two-wire interface must comply with the START and STOP conditions, as illustrated in the following Figure.



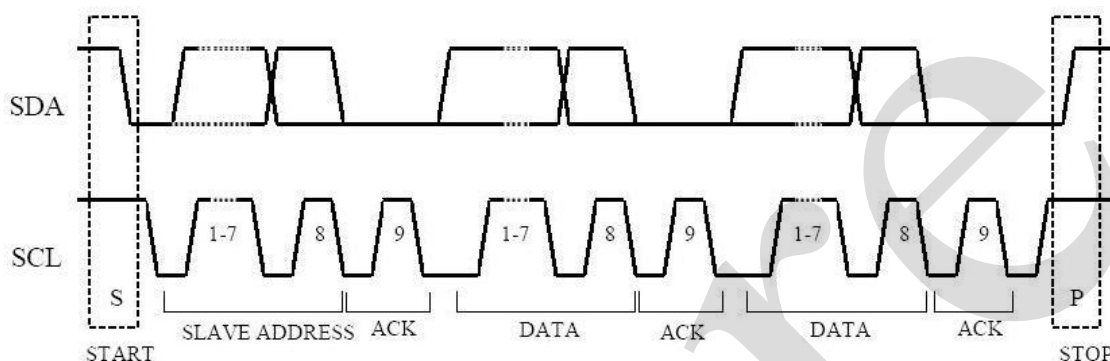
To input commands or display data to the BU9792 circuit, the following sequence must be strictly adhered to:

- ① START Condition
- ② Transmit Slave Address
- ③ Command/Data Transmission
- ④ STOP Condition



5.1.1、Acknowledge Signal (Acknowledge)

An acknowledge (Acknowledge) signal is required during actual data transmission. The transmitted data is composed of 8-bit units, and an Acknowledge signal is returned after the transmission of 8-bit data. After the transmission of 8-bit data (Slave Address, Command, Display Data), the SDA data line is released and an "L" signal is output when the 8th SCL signal falls. Then, the output stops when the 9th signal falls. However, the output is in the form of NMOS open-drain, and the H level is not output. When the Acknowledge signal is not required, input "L" from the falling edge of the 8th SCL signal to the falling edge of the 9th signal.



5.1.2、Command Transmission Mode

After the generation of the START condition, input the Slave Address ("01111100"), followed by a 1-byte command which must be input.

The MSB of the command determines whether the next set of data is a command or display data (the judgment bit for command or data).

Only when the judgment bit for Command or data is "1" can subsequent commands be input.

Only when the judgment bit for Command or data is "0" can subsequent display data be input.

S	Slave address	A	1	Command	A	1	Command	A	1	Command	A	0	Command	A	Display Data	...	P
---	---------------	---	---	---------	---	---	---------	---	---	---------	---	---	---------	---	--------------	-----	---

When in the state of inputting display data, command input is not allowed. If you want to input a command again, it is necessary to generate the start condition once more.

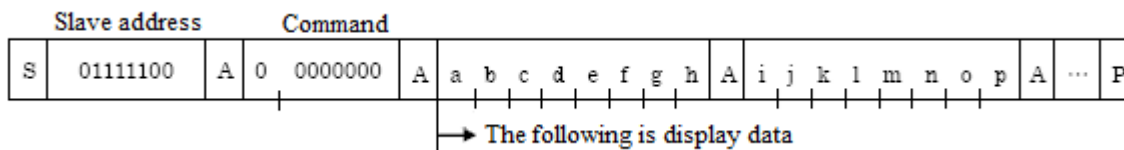
If a start condition or stop condition is input during command transmission, the command being transmitted will be canceled. When a start condition is input during transmission, the Slave Address must be input before switching to the command input state.

After the start condition is generated, the Slave Address data is transmitted first. If the initially transmitted Slave Address data is not recognized, no Acknowledge signal will be returned, and subsequent transmitted data will not be received. In the state where data reception is rejected, it will return to the state of inputting the start condition again.



5.1.3、Method of Writing and Transmitting Display Data

The BU9792 circuit has a built-in display data RAM (DDRAM) with a capacity of $36 \times 4 = 144$ bit. The corresponding relationship between the written display data and the address of the DDRAM data is as follows:



8-bit binary data is written into the DDRAM. The writing area is set by the Address Set command.

The address of every 4-bit data will automatically increment. Therefore, data can be continuously written into the DDRAM by sending consecutive data. The data written into the RAM is written once every 4 bits, so the operation of writing data will end if there is no action to wait for the Acknowledge signal.

	00H	01H	02H	03H		21H	22H	23H	
BIT0	a	e	i	m					COM0
BIT1	b	f	j	n					COM1
BIT2	c	g	k	o					COM2
BIT3	d	h	l	p					COM3
	SEG0	SEG1	SEG2	SEG3		SEG33	SEG34	SEG35	

5.2、Oscillation Circuit

The timing required for internal operations and liquid crystal display operations is generated by an oscillation circuit or an externally provided clock signal. The BU9792 circuit has a built-in oscillation circuit. When the built-in oscillation circuit is operating, the OSCIN pin is short-circuited to the VSS pin. When an external clock signal is provided, the switching is performed using the Set IC Operation (ICSET) command, and the external clock signal is input through the OSCIN pin.

5.3、LCD Bias Drive Circuit

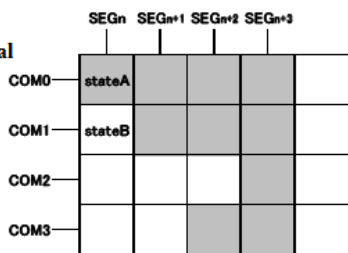
It generates liquid crystal driving voltages. Furthermore, a built-in BUFFER AMP enables low-power consumption for driving liquid crystal displays. The settings for 1/3 and 1/2 Bias are configured via the Mode Set (MODE SET) command. The setting for LINEFRAME inversion is configured through the Display Control (DISCTL) command.

Liquid crystal drive display waveform:



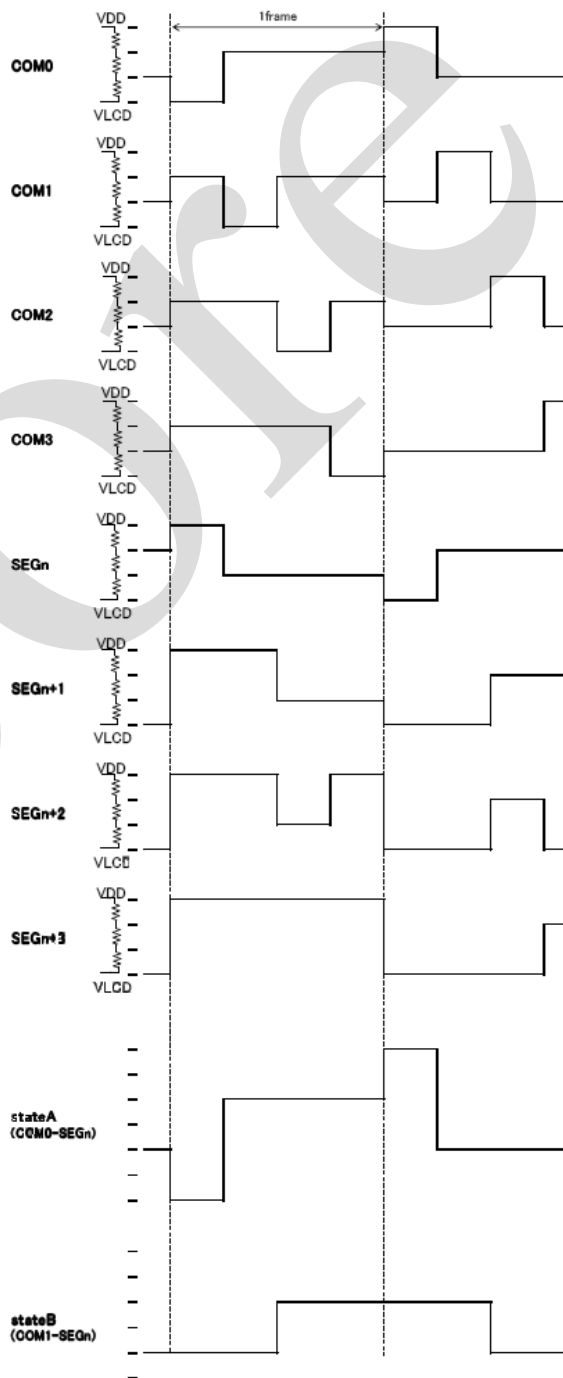
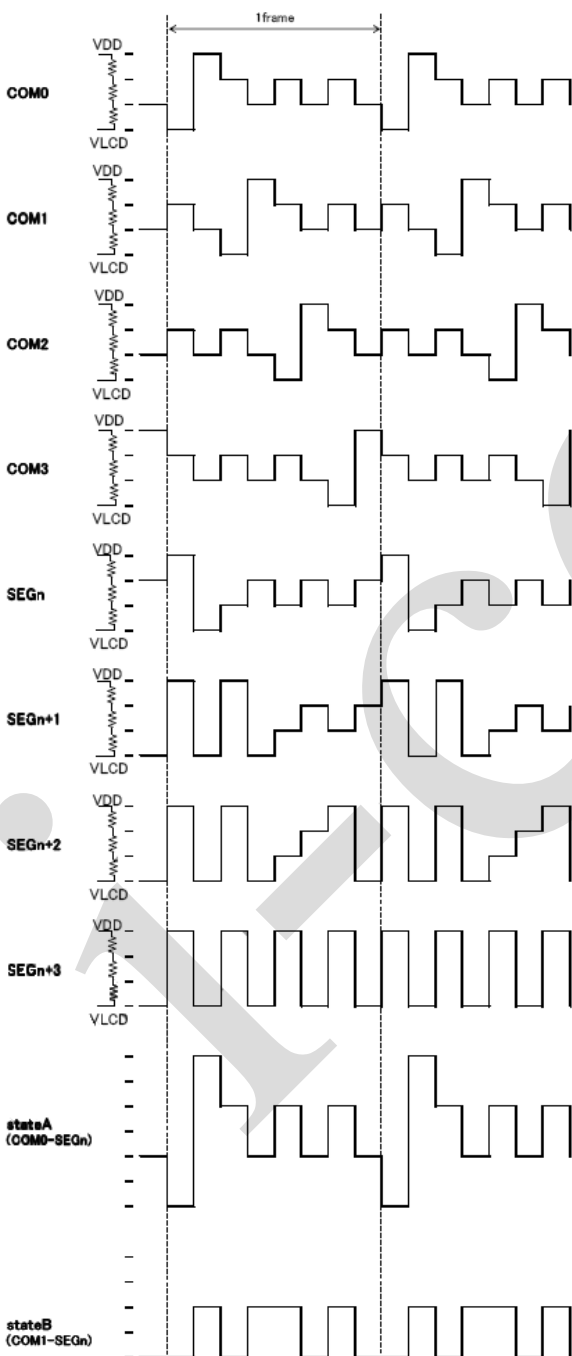
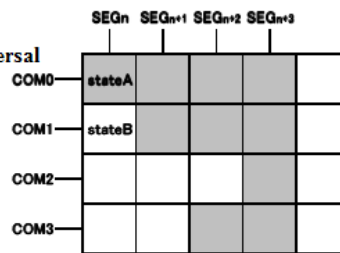
(1/3bias)

LINE Reversal



(1/3bias)

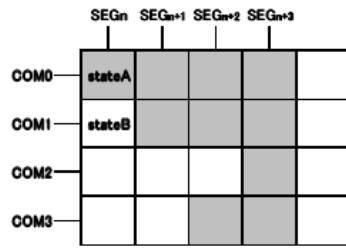
FRAME Reversal





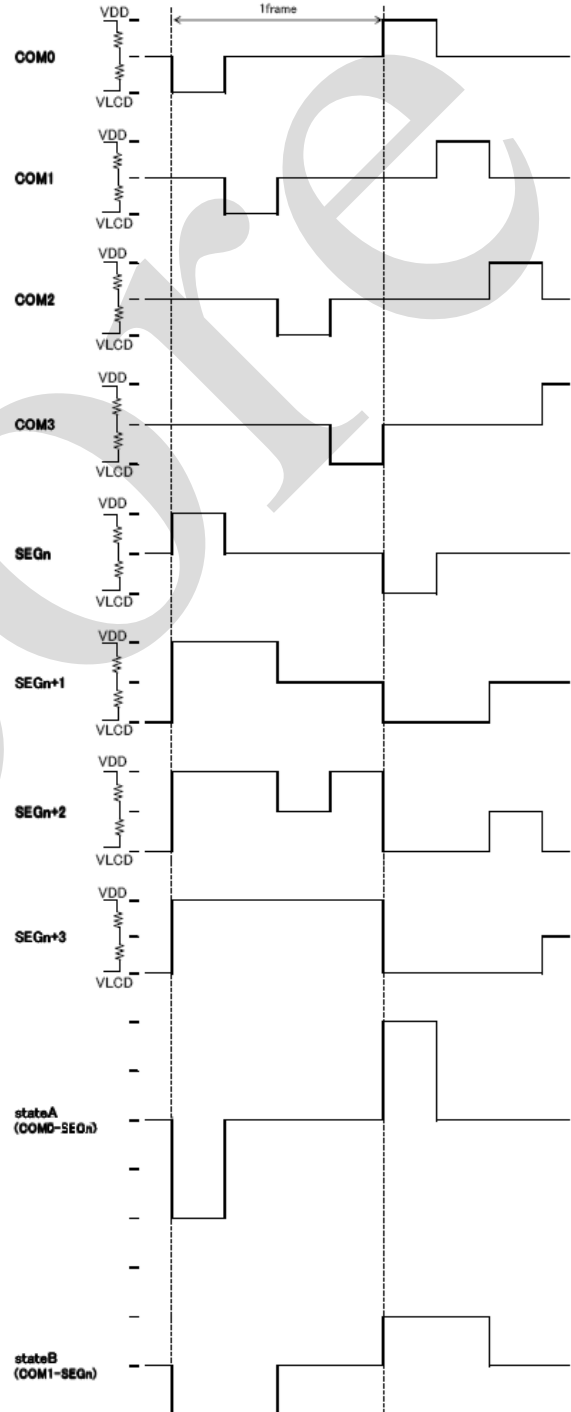
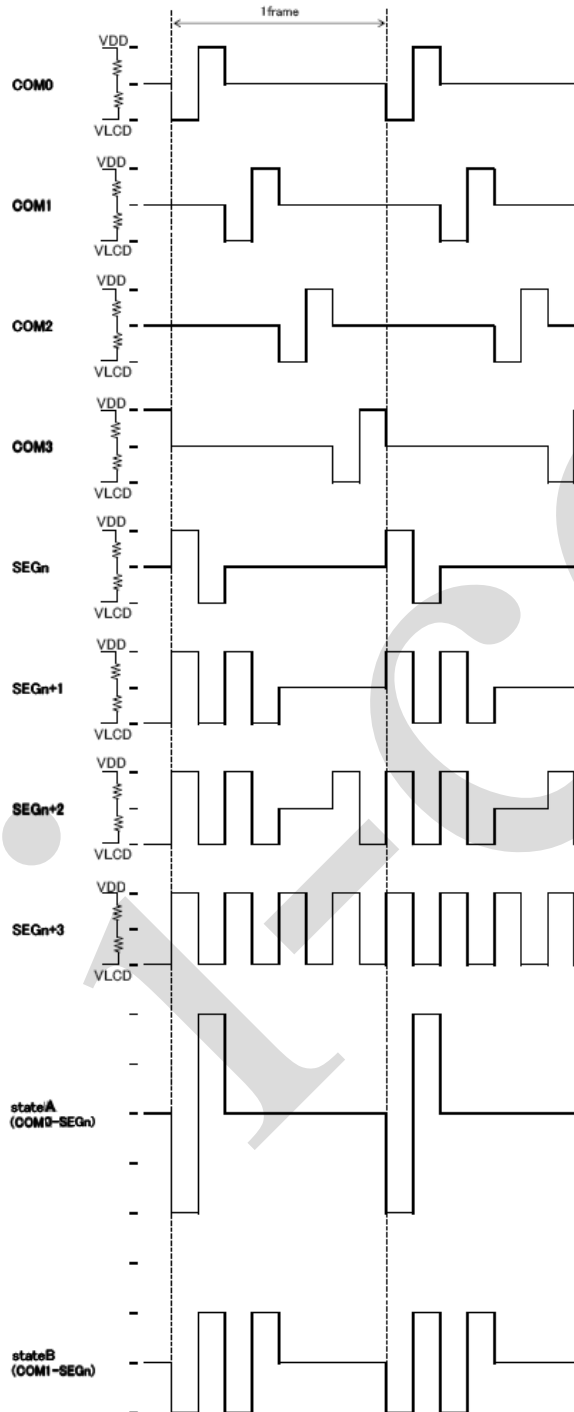
(1/2bias)

LINE Reversal



(1/2bias)

FRAME Reversal





5.4、Blinking Timing Generation

The BU9792 circuit has a built-in display blinking function. The setting of the blinking mode is configured via the Blink Control (BLK CTL) command.

When using the internal oscillation circuit, refer to the Blink Control (BLK CTL) command section for the blinking frequency.

When using an external oscillation circuit, the blinking frequency can be calculated based on the display frame frequency (f_{CLK}).

5.5、Initialization

5.5.1、Initialization Sequence

After power is applied, please perform the following steps to reset and initialize the circuit:

- Power on
- Stop condition
- Start condition
- Slave Address transmission
- Execute Software Reset according to the ICSEI command

Note: After power is applied, the values of each register and the DDRAM address are random until the initialization sequence is completed.

5.5.2、Reset Initialization State

The initial state of RESET after Software Reset is executed as follows:

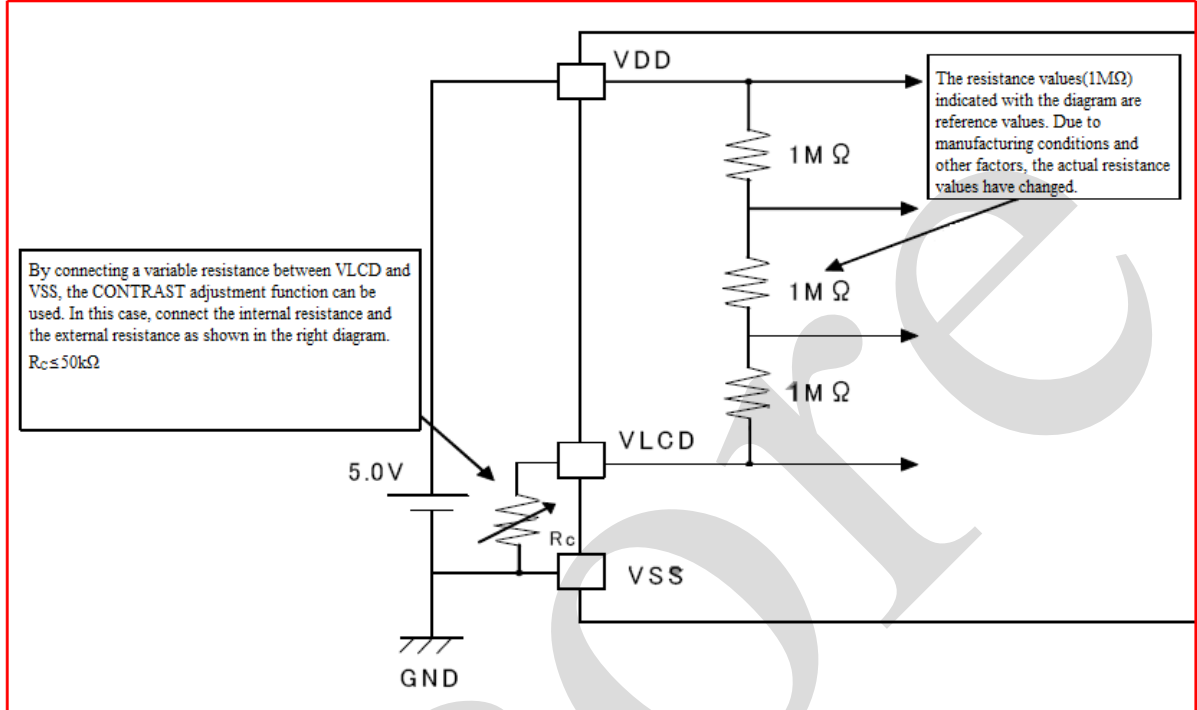
- The display is turned off.
- Initialize the DDRAM address (DDRAM data is not initialized).
- The initial values of the registers are described in detail in section 5.7 Command Description.



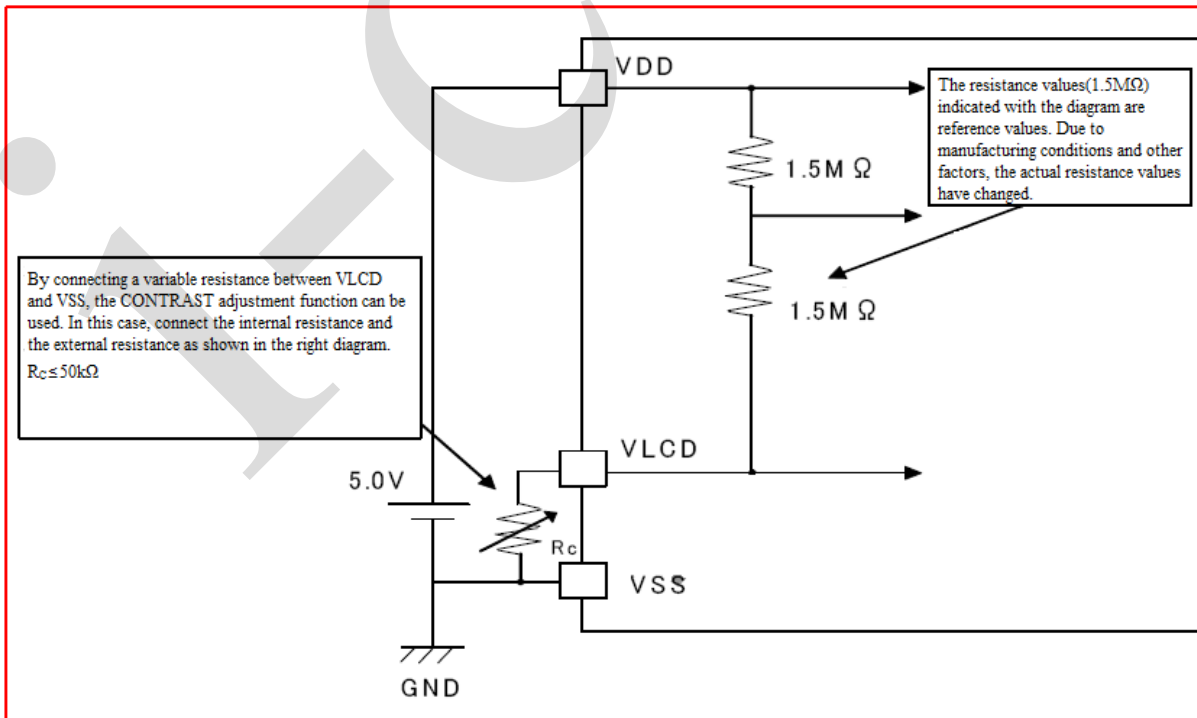
5.6、CONTRAST Adjustment Function

When using the CONTRAST adjustment function, since a variable resistor is connected between VLCD and VSS, the function of adjusting CONTRAST according to the variable resistance value can be utilized.

1/3Bias:



1/2Bias:



Note: When the CONTRAST function is not in use, directly short-circuit VLCD and VSS.



5.7、Command Description

D7 (MSB) is the judgment bit for commands or data. For detailed explanations, please refer to the two-wire serial interface commands and data transmission methods.

C: 0: The next Byte (D7-D0) is the data to be written into RAM.

1: The next Byte is a command

5.7.1、Mode Set (MODESET)

MSB								LSB
D7	D6	D5	D4	D3	D2	D1	D0	D0
C	1	0	*	D	BS	*		*

Setting Display ON/OFF:

Settings	D	Initial value
Display OFF	0	○
Display ON	1	—

Display OFF: Irrespective of the content in DDRAM, after writing DISPLAY OFF, all outputs of SEGMENT and COMMON will stop. The Display OFF mode is terminated upon inputting Display ON.

Display ON: The outputs of SEGMENT and COMMON become valid, and the read operation from DDRAM to the liquid crystal display starts.

Set Bias

setting	BS	Initial Value
1/3 Bias	0	○
1/2 Bias	1	—

According to the Bias setting, refer to the example diagram of the liquid crystal driving waveform for the output waveforms of SEG/COM.

5.7.2、Address set (ADSET)

MSB								LSB
D7	D6	D5	D4	D3	D2	D1	D0	D0
C	0	0	AD4	AD3	AD2	AD1		AD0

The address counter is set based on the address data specified by AD[4:0].

The settable address range is 00000~10011 (in binary). Values outside the above range are not allowed.

(If the set address exceeds the range, it will be set as "0".)

The ICSET command only sets the AD5 bit ("0" or "1") of the address and does not set the address itself.

The ADSET command must be input when setting the address.



5.7.3、Display control (DISCTL)

MSB							LSB	
D7	D6	D5	D4	D3	D2	D1	D0	
C	0	1	FR1	FR0	FM	SR1	SR0	

1、Setting Power save mode FR:

Power save mode FR	FR1	FR0	Reset Initialization State
Normal mode	0	0	○
Power save mode1	0	1	—
Power save mode2	1	0	—
Power save mode3	1	1	—

Note: The operating current decreases in the order of Normal mode>Power save mode 1>Power save mode 2>Power save mode 3.

2、Setting Liquid Crystal Driving Waveform

Setting	FM	Initial Value
LINE inversion	0	○
FRAM inversion	1	—

Note1: The operating current follows the order: LINE inversion>FRAME inversion.

Note2: For the driving methods of LINE inversion and DFRAME inversion, please refer to the liquid crystal driving waveform.

3、Setting Power save mode SR:

设定	SR1	SR0	Initial Value
Power save mode 1	0	0	—
Power save mode 2	0	1	—
Normal mode	1	0	○
High power mode	1	1	—

Note1: The operating current increases in the order: Power save mode 1<Power save mode 2<Normal mode<High power mode.

Note2: When using High Power Mode, ensure that the requirement $VDD-VLCD \geq 3.0V$ is met.

Refer to Consumption Current Data

Setting	Consumption Current
Power save mode 1	$\times 0.5$
Power save mode 2	$\times 0.67$
Normal mode	$\times 1.0$
High power mode	$\times 1.8$

The aforementioned consumption current data is a coefficient ratio based on normal mode, not absolute current values, and is for reference only. The proportional coefficient varies according to changes in the PANEL load.

Note3: The settings of Power save mode FR, liquid crystal driving waveform, and Power save mode SR mainly affect the following display quality. Please select the most appropriate values based on the current consumption and display quality of the LCD screen equipped with this chip.



Mode	Screen flicker	Display quality / contrast
Power save mode FR	○	—
Liquid crystal driving waveform	○	○
Power save mode SR	—	○

5.7.4、Set IC Operation(ICSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	1	AD5	RST	OSC

Execute Software Reset:

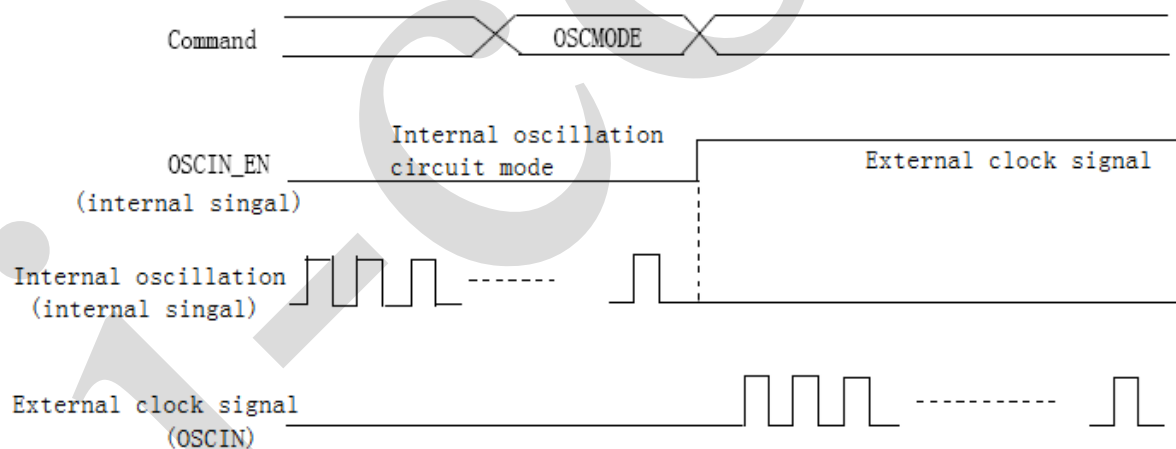
Setting	RST
Not Execute Software Reset	0
Execute Software Reset	1

When the Software Reset command is executed: The chip is reset to its initial state (refer to the RESET initial state).

OSC MODE	OSC	Initial value
Internal oscillation circuit	0	○
External clock signal input	1	—

When setting the built-in oscillation circuit: Please short-circuit the OSCIN pin to the VSS pin.

When setting external clock signal input: The external clock signal is input through the OSCIN pin.



OSCMODE Switch Timing



5.7.5、Blink control (BLKCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	*	BK1	BK0

Setting of blinking.

Blinking mode(Hz)	BK1	BK0	Initial value
OFF	0	0	○
0.5	0	1	—
1	1	0	—
2	1	1	—

5.7.6、All pixel control (APCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	1	AP	APN

Setting Full-Screen Lighting and Canceling Lighting:

APON	AP	Initial value
Normal	0	○
All pixel ON	1	—

APOFF	APN	Initial value
Normal	0	○
All pixel OFF	1	—

All pixels ON: Full-screen lighting is independent of the content in DDRAM.

All pixels OFF: Full-screen lighting cancellation is independent of the content in DDRAM.

The All pixels ON/OFF commands are only valid when the display is turned on (Display ON). At this time, the content of DDRAM remains unchanged.

Note: When both AP and APN are set to "1", APOFF takes priority.

5.8、Display Data Example

As shown in Figure 3 and Figure 4 are the segment bit positions of SEG/COM.

After the data shown in Table 1 is written into DDRAM, the characters in Figure 5 will be displayed on the LCD screen.

		SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19
COM0	D0	0	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0
	D1	0	0	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0



COM2	D2	0	0	0	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
		0	0	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
	COM3	0	0	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
		00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h	12h	13h

Table 1. DDRAM Data sheet

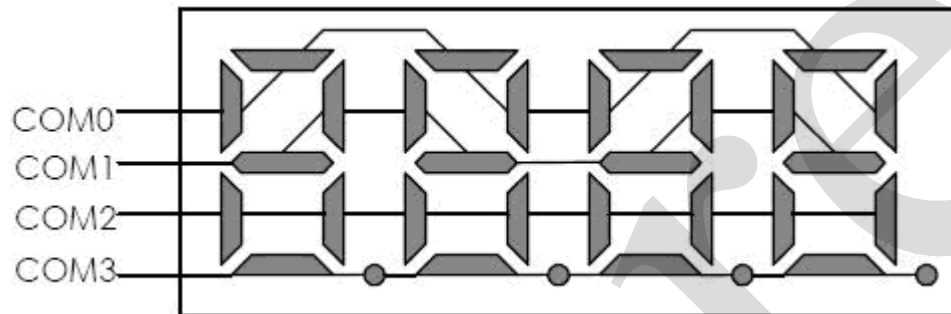


Figure 3. Example Diagram of COM - Segment Bit Positions

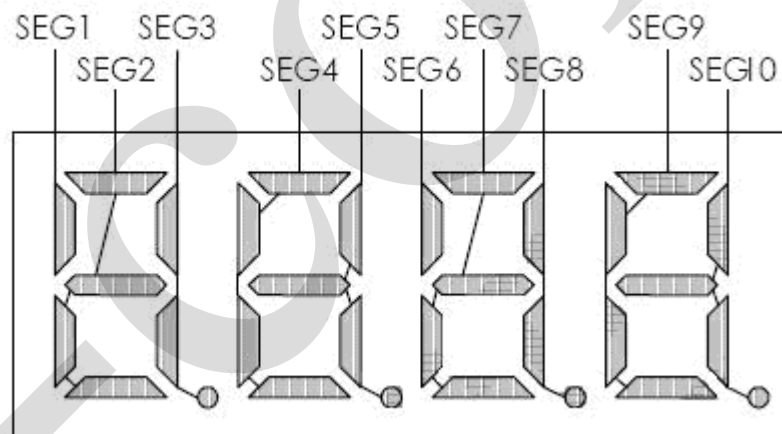


Figure 4. Example Diagram of SEG - Segment Bit Positions



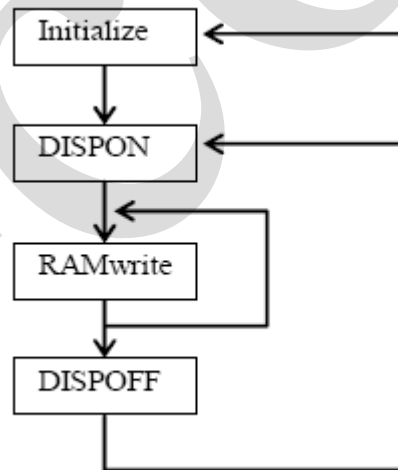
Figure 5. Example Diagram of Display Data



5.9、Timing

5.9.1、Start Timing IC Initialization

No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	Power on									VDD=0-5[V] (Tr=0.1[ms])
2	Wait 100us									IC Initialization
3	Stop									STOP condition
4	Start									START condition
5	Slave address	0	1	1	1	1	1	0	0	Transmit Slave address
6	ICSET	1	1	1	0	1	*	1	0	Software Reset
7	BLKCTL	1	1	1	1	0	*	1	1	Set BLKCTL
8	DISCTL	1	0	1	0	0	0	1	0	Set DISCTL
9	ICSET	1	1	1	0	1	0	0	1	AD5 setting of RAM address
10	ADSET	0	0	0	0	0	0	0	0	RAM address setting
11	Display Data	*	*	*	*	*	*	*	*	Address 00h-01h
	Display Data	*	*	*	*	*	*	*	*	Address 02h-03h
		*	*	*	*	*	*	*	*	
	Display Data	*	*	*	*	*	*	*	*	Address 22h-23h
12	Stop									STOP condition
13	Start									START condition
14	Slave address	0	1	1	1	1	1	0	0	Transmit Slave address
15	MODESET	1	1	0	*	1	0	*	*	Display On
16	Stop									STOP Condition





5.9.2、Initialization Timing

Input	D7	D6	D5	D4	D3	D2	D1	D0	Description
Power on									
Wait 100us									
STOP									
START									
Slave address	0	1	1	1	1	1	0	0	Transmit Slave address
ICSET	1	1	1	0	1	0	1	0	Software Reset
DISCTL	1	0	1	1	1	1	1	1	Set Display Control
ADSET	0	0	0	0	0	0	0	0	Set RAM address
Display Data	*	*	*	*	*	*	*	*	Display data
STOP									

5.9.3、Display On Mode Timing

Input	D7	D6	D5	D4	D3	D2	D1	D0	Description
START									
Slave address	0	1	1	1	1	1	0	0	Transmit Slave address
DISCTL	1	0	1	1	1	1	1	1	Set Display Control
BLKCTL	1	1	1	1	0	0	0	0	Set BLKCTL
APCTL	1	1	1	1	1	1	0	0	Set APCTL
MODESET	1	1	0	0	1	0	0	0	Display on
STOP									

5.9.4、Write RAM Data Mode Timing

Input	D7	D6	D5	D4	D3	D2	D1	D0	说明
START									
Slave address	0	1	1	1	1	1	0	0	Transmit Slave address
DISCTL	1	0	1	1	1	1	1	1	Set Display Control
BLKCTL	1	1	1	1	0	0	0	0	Set BLKCTL
APCTL	1	1	1	1	1	1	0	0	Set APCTL
MODESET	1	1	0	0	1	0	0	0	Display on
ADSET	0	0	0	0	0	0	0	0	Set RAM address
Display Data	*	*	*	*	*	*	*	*	Display on
STOP									

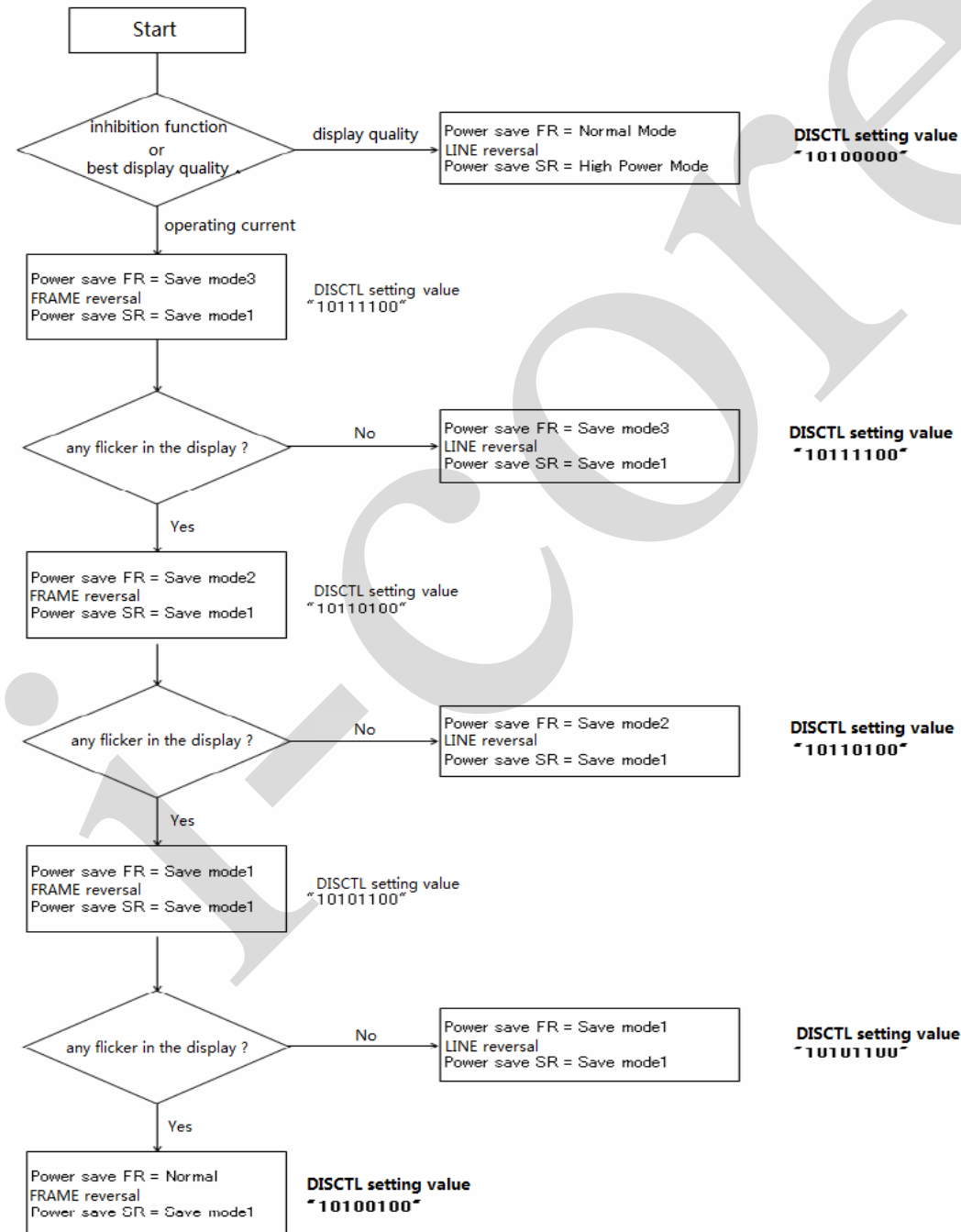


5.9.5、Display Off Mode Timing

Input	D7	D6	D5	D4	D3	D2	D1	D0	Description
START									
Slave address	0	1	1	1	1	1	0	0	Transmit Slave address
MODESET	1	1	0	0	0	0	0	0	Display Off
STOP									

5.9.6、DISCTL setting process

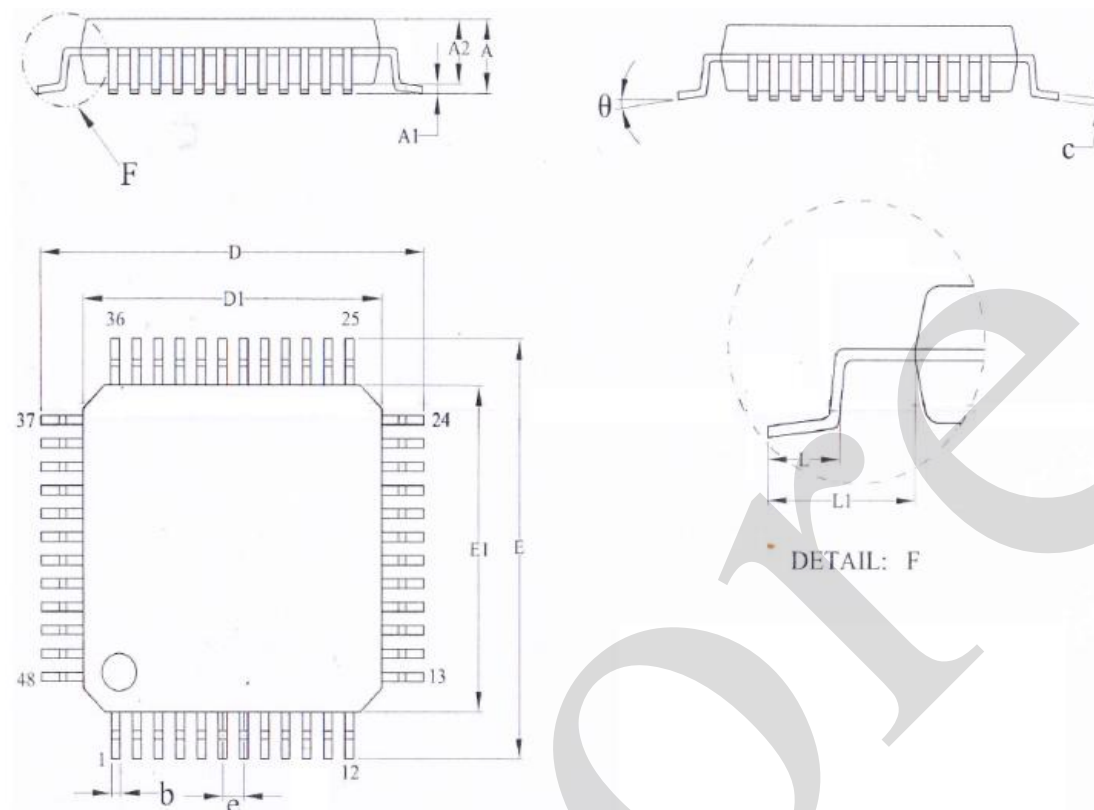
This is a flow chart for determining the setting value of the DISCTL command. Please refer to the following flow chart during configuration.





6、Package Information

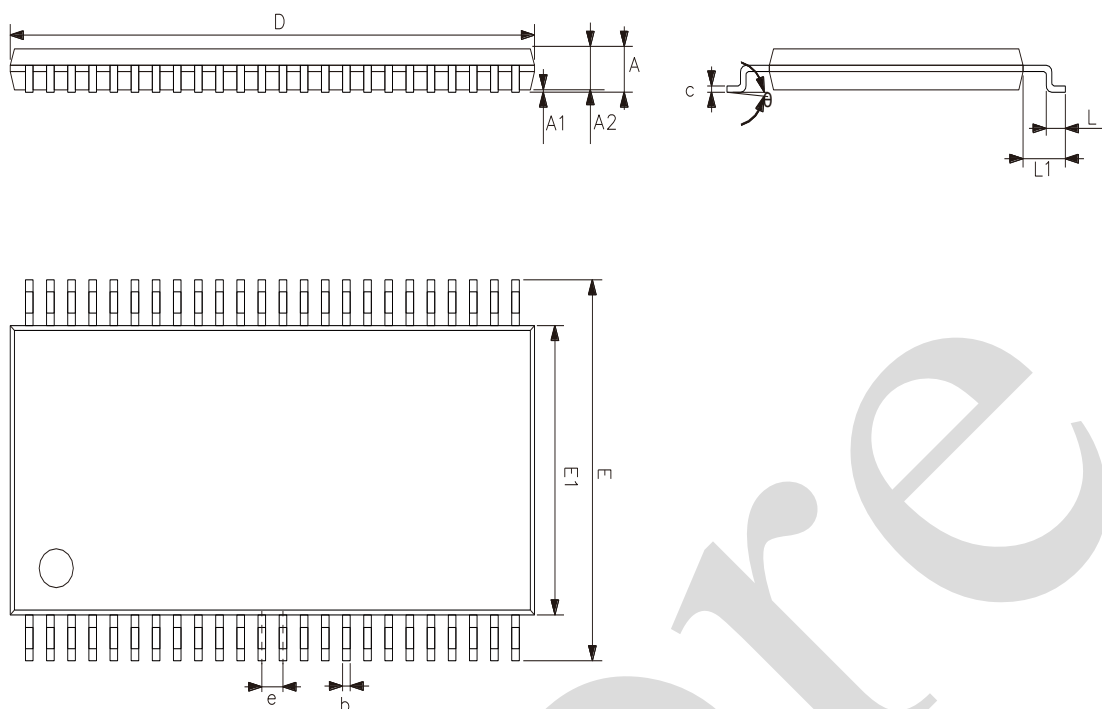
6.1、LQFP48



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	1.45	1.65
A1	0.05	0.20
A2	1.30	1.50
b	0.17	0.27
c	0.09	0.20
D	8.80	9.20
D1	6.90	7.10
E	8.80	9.20
E1	6.90	7.10
e	0.50	
L	0.43	0.80
L1	1.00	
θ	0°	10°



6.2、TSSOP48



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	—	1.20
A1	0.03	0.15
A2	0.82	1.05
b	0.17	0.27
c	0.12	0.22
D	12.40	12.60
E	7.90	8.30
E1	6.00	6.20
e	0.50	
L	0.35	0.75
L1	1.00	
θ	0°	8°



7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

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